Model 560-5900 PCI-SG
Model 560-5901 GPS PCI
Model 560-5901-1 GPS PCI
(with Down Converter)

PCI Plug-In Card

Generator
Synchronized Generator
GPS Synchronized Generator

SERIAL NUMBER _____

May 21, 2001
Revision G

TRUETIME

3750 Westwind Boulevard
Santa Rosa, California 95403

t 707.528.1230
f 707.527.6640
w www.truetime.com

FCC Notice and Compliance Statement

Model:

XL-DC, 151-600
XL-DC, 151-601
XL-DC, 151-601-178-1
XL-DC, 151-602
XL-DC, 151-650
XL-DC, 151-652
XL-DC, 151-652-382
GPS-PC, 560-5500
PC-SG2, 560-5503
GPS-VME, 560-5600
VME-SG2, 560-5608
PCI-SG, 560-5900
GPS-PCI, 560-5900-3
GPS-PCI, 560-5901
GPS-PCI, 560-5901-1
GPS-605, 820-501-000
NMC-100, 820-501-001
GPS-605, 820-501-003
RD-05, 820-500
NTS-90, NTS-305
NTS-90, NTS-405
NTS-90, 600-210
NTS-90, 600-310
NTS-90, 600-410
NTS-90, NIC-205
NTS-90, NIC-305
NTS-90, NIC-405
NTS-100, 600-201
NTS-100, 600-301
NTS-100, 600-401
NTS-100i, NIC-215
NTS-100i, NIC-315
NTS-100i, NIC-415
NTS-200-101 (48 VDC)
TIMEVAULT 6000-100
56000 DRC, 560-197-10

FCC Notice

This device has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a commercial installation. This device generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Caution: Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment.

FCC Compliance Statement

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

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Declaration of Conformity

Models:

PCI-SG, PCI Plug-In Synchronized Generator Card, 560-5900
GPS-PCI, PCI Plug-In GPS Synchronized Card, 560-5901

These products comply with the following European Union Directives:

89/392/EEC Safety of Machinery
as amended by 91/368/EEC, 93/44/EEC, 93/68/EEC

89/336/EEC Electromagnetic Compatibility
as amended by 92/31/EEC

73/23/EEC Low Voltage Safety
as amended by 93/68/EEC, 94/C199/03, 95/C214/02

91/157/EEC Accumulators and Batteries
as amended by 93/86/EEC

The following standards were used to verify compliance with the Directives:

EN55011 Class A, Group 1 & EN50082-1 (1997)

Conditions for Acceptability:

1. Must be installed in a CE-compliant chassis providing EMC and Safety protection similar to test conditions.
2. Must be provided CE-complaint extra-low voltage (ELV) power similar to test conditions.

Approved by

H. Pamiak, R&D Manager

H. Flesch, Marketing Manager

E. Rumphrey, Operations Manager

M. Von der Porten, Manager of Administrative Services

1 April 1999

TrueTime, Inc., 2835 Duke Court Santa Rosa, CA 95407 • Phone 707 528 1230 • Fax 707 527 6640 • E-Mail: truetime@nbn.com

NOTICE ON SCHEMATICS

Please be advised that there may or may not be references in the text of this manual to schematic drawings. TrueTime's general policy is to not include schematics because they may contain proprietary information. If you require copies of any schematic, please contact:

Customer Service
Service@Truetime.com
Phone: (707) 528-1230
Fax: (707) 527-6640

Addendum for 142-603
Antenna Downconverter Assembly

PHYSICAL SPECIFICATIONS

Antenna Downconverter Size:	4.4 in. dia. x 2.1 in. (11.17 cm. dia. x 6.85 cm.)

Note: Antenna DownConverter Units are mounted on a 12-inch long PVC nipple with a 3/4-inch Male Pipe Thread (MPT) on both ends. The above specified overall lengths of the Antenna DownConverter Units are therefore increased by approximately 11.25 inches, when the mounting nipple is included.

Antenna DownConverter Weight: (Including Mtg. Nipple)	0.60 lb (.272 Kg)
Antenna DownConverter Cable, RG-58:	Available lengths = 150 - 1500 ft. (standard length 50 ft.) 2.7 lb (1.23 Kg) per 100 ft.

ANTENNA CABLE DELAY ENTRY/REQUEST

The as shipped default antenna cable delay is +60 nS. **When the downconverted antenna is being used, 150 nS should be <u>added</u> to the cable delay entered.**

Addendum for 142-612
Antenna Assembly

PHYSICAL SPECIFICATIONS

Antenna Size:	2.625 in. dia. x 1.5 in. (6.67 cm. dia. x 3.81 cm.)

Note: The Antenna is mounted on a 12-inch long PVC nipple with a 3/4-inch Male Pipe Thread (MPT) on both ends. The above specified overall length of the Antenna. Units are therefore increased by approximately 11.25 inches when the mounting nipple is included.

Antenna Weight: (Including mtg. nipple)	0.55 lb (.250 Kg)
Antenna Cable, RG-59	Standard length = 50 ft. 1.2 lb (.545 Kg)
Optional Antenna Cable, RG-59	Available lengths to 200 ft. 2.7 lb (1.23 Kg) per 100 ft.

OPERATING SPECIFICATIONS

Antenna Power Regulated	+5 Volts DC @ <25mA
Antenna Frequency (L1)	1575.42 MHz
Code	Coarse Acquisition (C/A) Code

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:	-40° to +70°C (-40° to +158°F)
Storage Temperature:	-55° to +85°C (-67° to +185°F)
Humidity:	100%, condensing

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Declaration of Conformity

Models:

PCI-SG, PCI Plug-In Synchronized Generator Card, 560-5900
GPS-PCI, PCI Plug-In GPS Synchronized Card, 560-5901

These products comply with the following European Union Directives:

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as amended by 91/368/EEC, 93/44/EEC, 93/68/EEC

89/336/EEC Electromagnetic Compatibility
as amended by 92/31/EEC

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as amended by 93/68/EEC, 94/C199/03, 95/C214/02

91/157/EEC Accumulators and Batteries
as amended by 93/86/EEC

The following standards were used to verify compliance with the Directives:

EN55011 Class A, Group 1 & EN50082-1 (1997)

Conditions for Acceptability:

1. Must be installed in a CE-compliant chassis providing EMC and Safety protection similar to test conditions.
2. Must be provided CE-complaint extra-low voltage (ELV) power similar to test conditions.

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M. Von der Porten, Manager of Administrative Services

1 April 1999

TrueTime, Inc., 2835 Duke Court Santa Rosa, CA 95407 • Phone 707 528 1230 • Fax 707 527 6640 • E-Mail: truetime@nbn.com

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SECTION ONE

GENERAL INFORMATION

1.1 SCOPE OF MANUAL

This manual contains the information necessary to operate and maintain the TrueTime PCI-SG with the GPS Receiver option and available Down-Converter option. This timing card conforms to the PCI Local Bus Specification, Revision 2.1.

1.2 GENERAL DESCRIPTION

The PCI-SG functions as a Generator or Synchronized Generator supplying precise time (microseconds through thousands of years) to the host computer. In the Generator mode the time may be started, stopped, and preset via the PCI bus.

The Generator will phase lock to the GPS 1 PPS signal in the GPS Synchronized Generator mode. In the Synchronized Generator mode the Generator can phase lock to and decode an external time code signal. The internal oscillator is disciplined to remove any frequency offset with respect to the external reference. This is necessary to maintain precise phase lock and to minimize drift error during periods when the input reference is lost.

Time information and status are available via the PCI bus in three, 32-bit words. Each word contains packed-BCD time values. The data is immediately available (zero latency).

The user can capture the time in two different ways. The user may write to an address that latches the time in a set of registers. Alternately, an external event signal will latch the time in a second, independent set of registers permitting time tagging of an external event. The event can generate an interrupt to flag its occurrence and the time can then be read over the bus.

The user can configure a Rate Generator that will output pulsed signals with one of many available rates to a rear-panel connector. The generated signal may be configured to produce an interrupt to the PCI host processor. The user can also program a Time Compare pulse to output at a preset time.

The user can interrupt the PCI host processor using any of three sources: External Event, Rate Generator, and Time Compare.

1.3 PHYSICAL SPECIFICATIONS

The PCI-SG is a single-slot PCI-compatible short-card (6.875” long).

1.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are:

Operating Temperature:	0° to +50°C (+32° to +122°F)
Storage Temperature:	-17° to +100°C (0° to +212°F)
Humidity:	95% relative, non-condensing

1.5 POWER SPECIFICATIONS

The PCI host computer powers the unit. The typical input power specifications are:

PCI-SG Voltage:	+5 VDC @ 600 mA +12 VDC @ 24 mA - 12 VDC @ 47 mA
PCI-SG (GPS) with Antenna Voltage:	+5 VDC @ 840 mA +12 VDC @ 24 mA -12 VDC @ 47 mA
PCI-SG (GPS) with Down-converter/Antenna Voltage:	+5 VDC @ 840 mA +12 VDC @ 204 mA -12 VDC @ 47 mA

1.6 INPUT SIGNAL SPECIFICATIONS

GPS Reference

Phase Accuracy:	< 1 microsecond to UTC
Phase Correction:	Step size 60 ns, after phase lock
Position Accuracy:	Latitude, longitude, and elevation 25 meters SEP without SA
Acquisition Time:	5 minutes on cold start
Receiver Input:	
Frequency:	1575.42 MHz (L1)
Code:	Coarse Acquisition (C/A)
Tracking:	6 satellites (4 for solution)
Local Offset:	±12:59 and DST
Connector:	Rear panel female BNC "ANTENNA"

Amplitude-Modulated Reference Code Input

Format:	Amplitude-modulated IRIG-B122 or Amplitude-modulated IRIG-A132
Amplitude:	0.5 to 10 Vpp
Impedance:	Selectable, 10k Ω, 600 Ω or 50 Ω to GND
Ratio:	2:1 to 5:1
Error Bypass:	3 frames
Phase Accuracy:	<5 µs with stable reference
Phase Correction:	Step size 60 ns, after phase lock

Phase Compensation:	±1 ms in 1 µs steps
Tracking Range:	$5x10^{-6}$ necessary to meet frequency discipline specification (Section 1.8) and lock requirements
Connector:	Rear-panel female BNC "CODE IN"

DC-shift Reference Code Input

Format:	DC-shift IRIG-B002 or DC-shift IRIG-A002
Levels:	RS-422 or TTL
Impedance:	
Jumper-Select:	120 Ω or HI (4K Ω minimum)
Error Bypass:	3 frames
Phase Accuracy:	<5 µs with stable reference
Connector:	Rear-panel 9-pin D subminiature Pin 3(+), 4(-) for RS-422 levels Pin 3(SIG), 2(GND) for TTL levels

External 1 PPS Reference Input

Active Edge:	Rising
Levels:	
Logic 0:	-0.5 to +1.75 VDC
Logic 1:	+2.25 to 5.0 VDC
Impedance:	Approximately 2k Ω
Phase Accuracy:	<1 µs, typically <500 ns with stable reference
Connector:	Rear panel 9-pin D subminiature, pin 1

External Event Input

Active Edge:	Rising
Levels:	
Logic 0:	-0.5 to +1.75 VDC
Logic 1:	+2.25 to 5.0 VDC
Impedance:	Approximately 2k Ω
Connector:	Rear-panel 9-pin D subminiature, pin 1

1.7 OUTPUT SIGNAL SPECIFICATIONS

Amplitude-modulated Generator Code Output

Format:	IRIG-B 122
Amplitude:	Adjustable, 0 to 10 Vpp into 600 Ω to ground
Ratio	Fixed, 3:1
Connector:	Rear-panel female BNC "CODE OUT"

DC-Shift Generator Code Output

Format:	DC-Shift IRIG-B002
Levels:	RS-422

Connector:	Rear-panel 9-pin D subminiature, pin 8(+), pin 9(-)

Time Compare Output

Resolution:	1 µs
Pulse Width:	Usually 2 ms (see Section 2.3.9)
Compare Mask:	Milliseconds through hundreds of days
Levels:	HCTTL
Timing:	Rising edge at time in Time Compare registers
Connector:	Rear-panel 9-pin D subminiature, pin 6

1 PPS Output

Rate:	1 PPS
Duty Cycle:	50%
Amplitude:	HCTTL
Timing:	Rising edge on-time
Connector:	Rear-panel 9-pin D subminiature, pin 5

Rate Generator Output

Timing:	Rising edge on-time
Rate:	10 KPPS, 1 KPPS, 100 PPS, 10 PPS, or 1 PPS
Levels:	HCTTL
Connector:	Rear-panel 9-pin D subminiature, pin 7

1.8 TIMING SPECIFICATIONS

Timing Accuracy:	Within 2 µs of code input time in Synchronized Generator mode. Within 1 µs to UTC-USNO in GPS Synchronized mode. Within 500 ns of external 1 PPS in Synchronized Generator mode.
Internal Oscillator:	
Frequency:	16.368 MHz
Stability:	±2.5 PPM, -30° to +75°C
Aging:	< 1 PPM/Year
Frequency Discipline:	<1x10E-7, typical 5x10E-8
Leap Year Reset:	Automatically resets to day 1 after day 365 standard years and after day 366 in leap years
Leap Second:	Automatically handles leap seconds in GPS Synchronized mode. User programmable on day of occurrence in Synchronized Generator mode.

1.9 GENERAL SPECIFICATIONS

Interrupts: Single PCI Interrupt

Configuration: The PCI-SG is configured at the factory. This can be changed anytime by the user. The PCI-SG with GPS option is configured for GPS Synchronized mode with no local offset. Also, the amplitude-modulated reference code input phase error has been zeroed using the Synchronized Generator Offset Register.

Jumpers:

JP1 Termination for RS-422 DC-shift reference code input.
JP1-1 and JP1-2 for 100Ω to 150Ω differential (RS-422) impedance, for 50Ω to 75Ω single-ended TTL impedance or when no input is connected.
Uninstalled for high differential or single-ended TTL impedance.

JP2 Termination for Amplitude Modulated reference code input.
JP2-1 and JP2-2 (600 Ω to GND)
JP2-2 and JP2-3 (10K Ω to GND)
JP2-3 and JP2-4 (50 Ω to GND)

JP3 Antenna voltage.
JP3-1 and JP3-2 (0V)
JP3-2 and JP3-3 (5V)
JP3-3 and JP3-4 (12V, used with down converter option)

I/O Connector: The I/O connector is a 9-pin male D connector mounted on the rear shield plate.

See Table 1-1 for pin assignments.

TABLE 1-1
USER I/O CONNECTOR PIN ASSIGNMENT

PIN	ASSIGNMENT
1	EXTERNAL EVENT INPUT
2	GND
3	DC REFERENCE CODE INPUT + OR TTL
4	DC REFERENCE CODE INPUT -
5	1 PPS OUTPUT
6	TIME COMPARE OUTPUT
7	RATE GENERATOR OUTPUT
8	DC GENERATOR CODE OUTPUT +
9	DC GENERATOR CODE OUTPUT -

1.10 ANTENNA SPECIFICATIONS

To operate in the GPS Synchronized Generator mode, the unit requires an external antenna input. This input can be supplied with a disk antenna, 142-601. Cable lengths from 200 to 1,000 feet require the antenna/downconverter option, 142-602.

The specifications for the 142-601 disk antenna are:

Size:	2.625 in dia. x 1.5 in (6.67 cm dia x 3.81 cm)*
Weight:	0.70 lb (.318 Kg) (incl. mtg. nipple)*
Operating Temperature:	-40° to +70° C (-40° to +158° F)
Storage Temperature:	-55° to +85° C (-67° to +185° F)
Humidity:	100% condensing
Power:	25 mA @ 5V (supplied by unit)

The specifications for the optional 142-602 disk antenna/downconverter are:

Size:	2.625 in dia. x 8.6 in (6.67 cm dia x 21.84 cm)*
Weight:	2.35 lb (1.067 Kg) (incl. mtg. nipple)*
Operating Temperature:	-40° to +70° C (-40° to +158° F)
Storage Temperature:	-55° to +85° C (-67° to +185° F)
Humidity:	100% condensing
Power:	180 mA @ 12V (supplied by unit)

* Note: Antenna and antenna/downconverter units are mounted on a 12-inch long PVC nipple with 3/4-inch Male Pipe Thread (MPT) on both ends. The above specified weights include this mounting nipple and the above specified sizes should be increased by approximately 11.25 inches when the mounting nipple is included.

1.11 CABLE SPECIFICATIONS

The basic unit is supplied with 50 feet of coaxial cable. Longer lengths are available from TrueTime. Cable lengths from 200 to 1,000 feet require the antenna/downconverter option.

Disk antenna 142-601 cable specifications:

Type:	RG-59
Length:	50 feet
Weight:	1.2 lb (.545 Kg)
Humidity:	All weather, outdoors
Connectors:	TNC male to BNC male

Optional disk antenna/downconverter 142-602 cable specifications:

Type:	RG-58
Length:	200 feet
Weight:	5.4 lb. (2.452 Kg)
Humidity:	All weather, outdoors
Connectors:	TNC male to BNC male

1.12 LIMITED WARRANTY

Each new product manufactured by TrueTime is warranted for defects in material or workmanship for a period of one year from the date of shipment ("Limited Warranty"). Defects in material or workmanship found within that period will be replaced or repaired, at TrueTime's option, without charge for material or labor, provided the customer returns the equipment, freight prepaid, to the TrueTime factory under this limited warranty. TrueTime will return the repaired equipment, freight prepaid, to the customer's facility. This one-year Limited Warranty does not apply to any software or to any product not manufactured by TrueTime. If on-site warranty repair or replacement is required, the customer will be charged the then-current field service rate for portal-to-portal travel time plus actual portal-to-portal travel charges. There is no charge for on-site warranty repair labor.

Products not manufactured by TrueTime but included as integral parts of a system (e.g. peripherals, options) are warranted for 90 days or longer, as provided for by the original manufacturer, from the date of shipment. Aside from the Limited Warranty set forth above, TrueTime makes no other warranties, express or implied, of merchantability, fitness for purpose or of any other kind of description whatsoever.

By purchasing any product manufactured by TrueTime, the buyer consents to and agrees with TrueTime that as a result of the exclusion of all warranties, expressed or implied, or merchantability, fitness for purpose, or otherwise, except for the limited one-year warranty for defects in material and workmanship for products manufactured by TrueTime, that the Buyer has the sole responsibility to assess and bear all losses relating to (1) the ability of the product or products purchased to pass without objection under the contract description among merchants and buyers in the trade; (2) the conformity of the product or products to fair average quality within its contract description; (3) the fitness of the product for the ordinary purposes for which such product is used; (4) the consistency of quality and quantity within each unit of product or products and among all units involved; (5) the adequacy of containers, packaging and labeling of the product or products; (6) the conformity of the product, promises or affirmations of fact (if any) made on its label or container; and (7) the conformity of the product to standards of quality observed by other merchants in the trade with respect to products of similar description.

1.13 LIMITATION OF LIABILITY

By purchasing any product from TrueTime the Buyer consents to and agrees that the Buyer's sole and exclusive remedy for any damages or losses incurred by the Buyer as a result of TrueTime's breach of its one-year Limited Warranty for defects in materials and workmanship or otherwise in connection with any claim respecting the product shall

be limited to the repair or replacement of the product or a refund of the sales price of the product.

In no event shall the Buyer be entitled to recover consequential damages or any other damages of any kind or description whatsoever.

1.14 PROPRIETARY NOTICE

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SECTION TWO

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section contains installation instructions and operating procedures for the PCI-SG.

2.2 INSTALLATION

Unpack the unit and carefully inspect it for shipping damage. Any damage must be reported to the carrier immediately.

Record the serial number and the phase compensation value (located on a label on the Xilinx IC, on the card) in a safe place for later use.

The phase compensation number must be added algebraically to any known system delays (cable, distribution amps, deliberate offsets, etc.) and entered into the synchronized generator offset register as described in paragraph 2.3.4.1.1 in order for the card to meet its published accuracy spec. Note that this value is a factory measurement of delays through the card, as described in the above named paragraph.

With the power OFF, mount and secure the PCI-SG card in an empty PCI card slot. Fabricate any required I/O cables and connect them to the appropriate connectors. If using the GPS option, place the antenna with an unobstructed view of the sky.

2.3 OPERATION

The following paragraphs describe the operation of the standard PCI-SG. They describe the operating modes, the various registers used, and how to control and configure the card. All register addresses are specified as an offset from the PCI Memory Base Address. The following page is a summary of the PCI-SG mapping.

2.3.1 TIMING CARD REGISTERS

Data registers, mapped into PCI Memory Space, are used to control and configure the PCI-SG and report information. The use and function of these registers will be described in detail later in this section. These registers are briefly described as follows:

1. The Time and Position Freeze Registers are updated by writing to the low-order Freeze Register. The new values can be read immediately (zero latency). The Time registers contain year through unit microseconds. The Position Registers, used only in the GPS Synchronized mode, contain the GPS position (longitude, latitude, and elevation).

2. The Configuration Register controls the configuration of the PCI-SG card. It is used to select the mode of operation, to select the Synchronized Generator reference, to start and stop the Generator, to preset the Generator time, to preset GPS position, to set External Event input polarity, to select IRIG input/output

codes, select IRIG input source, to set the Rate Generator output and to set an initial position for the GPS receiver.

3. The Local Offset Sign Register and Local Offset Hours Register are used to convert UTC time to local time and are used in GPS Synchronized mode.

4. The DST Registers are used to tell the unit which days of the year to enter and exit Daylight Savings Time (DST).

5. The Synchronized Generator Offset Register is used to adjust the phase difference between the Synchronized Generator amplitude-modulated reference code and the time outputs to compensate for systematic delays.

6. The Diagnostic Register contains the results of the internal diagnostic tests performed at power-up and during normal operation.

7. The External Event Time Registers are used to retain the time an external event.

8. The Time and Position Preset Registers are used to preset the Generator time or preset a new position when in the GPS Synchronized mode.

9. The Time Compare Registers are used to program the Time Compare pulse output.

10. The Signal Level Registers contain the satellite numbers and signal levels of up to six satellites when in the GPS Synchronized mode.

11. The Hardware Control and Hardware Status Registers handle PCI-SG interrupt sources and status flags for external event, time compare, generator rate pulse, and antenna open/short.

2.3.1.1 STORED CONFIGURATION

Several parameters are retained in Electrically Eraseable Programmable Read Only Memory (EEPROM) while the PCI-SG power is off. These parameters define the configuration of the PCI-SG. They are the local offset, the rate generator output, the synchronized generator offset, the current year, the operating mode, synchronized generator reference, and the daylight savings time flag.

2.3.2 OPERATION MODES

The PCI-SG operates as either a stand-alone Generator or a Synchronized Generator. As a Synchronized Generator, the card can synchronize to a time code signal, to an external 1 PPS, or to GPS.

The PCI-SG is shipped with Synchronized Generator mode and IRIG-B AM selected. The PC-SG with GPS option is shipped with GPS Synchronized mode selected.

Mode Select. Select the mode by writing to the Mode Select bit of the Configuration Register (Section 2.3.13). Clearing this bit selects the Generator mode. No external

time reference is used in this mode. Setting the Mode Select bit means the Generator will synchronize to an external reference.

Reference Select. Select the Synchronized Generator time reference by writing to the Time Reference Select bits of the Configuration Register (Section 2.3.13). These bits allow selection between Input Code, GPS, and 1 PPS via the External Event Input.

2.3.3 GENERATOR MODE

In the Generator mode an internal time base generates time elapsed from power-up. The initial time may be preset and the accumulation of time may be started or stopped via the Configuration Register.

2.3.3.1 START/STOP

The Generator accumulates time when the Generator Stop bit of the Configuration Register is clear. The Generator stops when this bit is set. This bit is valid only in Generator mode.

2.3.3.2 PRESET TIME

The three locations shown in the table below are used to preset the Generator time. First, write the preset time (milliseconds through thousands of years) into the Preset Registers. Table 2-1 shows the data and offset of each register. Write packed BCD data to each register. Then set the Preset Time Ready bit of the Configuration Register. This bit will automatically clear once the preset time is loaded.

TABLE 2-1
PRESET TIME REGISTERS

	DATA								OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Time	0				0				0x158	0x158
Time	Units milliseconds (BCD)				0				0x159	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x15A	
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x15B	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x15C	0x15C
Time	Tens hours (BCD)				Unit hours (BCD)				0x15D	
Time	Tens days (BCD)				Unit days (BCD)				0x15E	
Time	0				Hundreds days (BCD)				0x15F	
Time	Tens years (BCD)				Unit years (BCD)				0x160	0x160
Time	Thousands years (BCD)				Hundreds years (BCD)				0x161	
Time	0				0				0x162	
Time	0				0				0x163	

2.3.3.3 TIME CODE OUTPUT

The Output Time Code is IRIG B AM or DC. AM Code is available at the "CODE OUT" BNC connector. DC Code is available at RS-422 levels via the DB-9 connector.

2.3.3.4 READ TIME

Writing to offset 0xFC will freeze the current time-of-day in the Time Freeze Registers. The registers may be read immediately and will remain static until the next freeze command. The Time Registers start at offset 0xFC. They contain packed BCD data, except for the Status bits. Table 2-2 shows the location of the Time Registers.

TABLE 2-2
TIME FREEZE REGISTERS

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Time	Tens microseconds (BCD)				Unit microseconds (BCD)				0xFC	0xFC
Time	Unit milliseconds (BCD)				Hundreds microseconds (BCD)				0xFD	
Time	Hardware Status Register[1]				Not Defined				0xFE	
Time	Not Defined				Not Defined				0xFF	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x100	0x100
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x101	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x102	
Time	Tens hours (BCD)				Unit hours (BCD)				0x103	
Time	Tens days (BCD)				Unit days (BCD)				0x104	0x104
Time	Status[2]				Hundreds days (BCD)				0x105	
Time	Tens years (BCD)				Unit years (BCD)				0x106	
Time	Thousands years (BCD)				Hundreds years (BCD)				0x107	

Note 1. See Section 2.3.11
Note 2. Status Bits:
B6 - 1 Indicates Phase Locked to Input Code or External 1 PPS.
B5 - 1 Indicates Time Code or External 1 PPS Input Valid.
B4 - 1 Indicates Locked to GPS.

2.3.4 SYNCHRONIZED GENERATOR MODE

The Synchronized Generator operates as a Generator that is synchronized to an external time reference. The Synchronized Generator phase locks to the time reference and disciplines the oscillator to remove frequency errors. The phase-correction logic maintains phase lock by advancing or retarding the time in 60 ns steps. If the reference code is lost, the Synchronized Generator continues to increment time based upon the disciplined internal time base. See Section 2.3.3.4 to read the time.

2.3.4.1 TIME CODE INPUT

Select the Time Code Input via the Code Register. The source can be selected from IRIG A AM Code, IRIG B AM Code, IRIG A DC Code, and IRIG B DC Code. The DC Code Input can be either RS-422 or TTL, depending on how the input connector is

wired. To use RS-422 logic levels, input DC-shift code at pins 3(+) and 4(-) of the 9-pin connector. If it is desired to use the optional 120 ohm termination resistor, move the jumper at JP1 to pins 1 and 2. To use TTL logic levels, connect DC-shift time code to pin 3 of the 9-pin connector. Make sure the jumper at JP1 is removed or parked on pin 1. Connect amplitude-modulated time code at the rear panel BNC labeled "CODE IN". Match the impedance of the input code using JP2 (Section 1.9).

TABLE 2-3
CODE REGISTER

DC-SHIFT INPUT CODE SELECTION		OUTPUT CODE SELECTION		INPUT CODE SELECTION		OFFSET	
BIT 7		BITS 6,5,4		BITS 3,2,1,0		BYTE	DWORD
0	Amplitude Modulated	0	IRIG-B	0	IRIG-B		
1	DC-Shift	1-17	Reserved	1	IRIG-A		
				2-15	Reserved		

2.3.4.1.1 PHASE COMPENSATION

When the Synchronized Generator is using amplitude-modulated time code as the reference, there are inherent delays caused by signal distribution amplifiers or transmission media. The reference code is input to the automatic gain control (AGC) circuit and then to the zero crossing detector. Both of these circuits can contribute small delays (less than 40 microseconds). Use the Synchronized Generator Offset to set the phase compensation value. This value will be used to offset fixed phase errors, either positive or negative. The value written must be a sixteen-bit signed binary number representing microseconds of compensation. The range of compensation is from -1000 to +1000 us. A magnitude larger than 1000 us will be ignored.

TABLE 2-4
SYNCHRONIZED GENERATOR OFFSET REGISTER

DATA									OFFSET	
DESCR	B7	B6	B5	B4	B3	B2	B1	B0	BYTE	DWORD
Offset	Offset - Lo								0x124	0x124
Offset	Sign	Offset - Hi							0x125	
Offset	0								0x126	
Offset	0								0x127	

2.3.4.1.2 PRESET YEAR

Year information is not encoded in the time code reference but is available over the PCI bus. To set the year use the Generator Time Preset function described in Section 2.3.3.2. Year data is necessary to handle end of year rollover correctly for leap years. Year information is saved in EEPROM and automatically increments at the end of each year.

2.3.4.2 EXTERNAL 1 PPS INPUT

The Synchronized Generator can synchronize to an external 1 PPS. To select this mode use the mode and reference select bits in the control byte of the configuration register (see Section 2.3.13.1). Since the reference contains no time information, set the time using the Time Preset function described in Section 2.3.3.2.

2.3.4.3 LEAP SECOND

To cause a leap second at the end of the day in Synchronized Generator Mode, set bit 1 of the Configuration Register #2 at offset 0x12C. The unit will add an extra second at the end of the current day. Bit 1 of Configuration Register #2 will clear automatically after the leap second as occurred.

2.3.5 GPS SYNCHRONIZED MODE

In the GPS Synchronized Generator mode the card operates with the GPS Module. Select GPS as the time reference via the Configuration Register (Section 2.3.13). The GPS Module receives transmissions from the NAVSTAR Global Positioning Satellite system and derives time that is traceable to the National Institute of Standards and Technology (NIST). If the GPS Module indicates that good time is available, the card will transfer GPS time into the generator time registers. The card will phase lock to the GPS Module 1 PPS and discipline the oscillator. Phase errors are removed by the phase correction logic that advances or retards the generator time using 60 nanosecond steps. When the card is within the timing specifications (defined in Section 1.9), the Locked to GPS flag will be set in the Time Register. With satellites visible, the card will normally lock within 20 minutes.

The GPS Module assumes a moderate dynamic environment (LAND mode, velocity <120 knots). The fix mode is AUTO 2-D/3-D and is preferable for most land applications.

2.3.5.1 LOCAL OFFSET

The value stored in the Local Offset Registers are used to convert UTC-USNO to local time. The range of the local offset is from -12:59 to +12:59 hours. The data is in packed BCD format. Table 2-5 shows the location of the data. These registers are used in the GPS Synchronized mode.

TABLE 2-5
LOCAL OFFSET REGISTERS

DATA								OFFSET	
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Tens minutes (BCD)				Unit minutes (BCD)				0x120	0x120
Tens hours (BCD)				Unit hours (BCD)				0x121	
Sign Byte-- ASCII '-' (0x2D) / ASCII '+' (0x2B)								0x122	
0								0x123	

2.3.5.2 DAYLIGHT SAVING TIME

In the GPS Synchronized Generator mode, the card provides the ability to automatically handle the DST transitions. The transition takes place at 2:00 a.m. local time on the first Sunday in April and the last Sunday in October. To enable this feature, set the DST bit in the Configuration Register (Section 2.3.13).

2.3.5.3 READ TIME/POSITION

In the GPS Synchronized mode, both time and position are available over the PCI bus. Writing to offset 0xFC will freeze the current time-of-day and current position in the Time/Position Freeze Registers. The registers may be read immediately and will remain static until the next freeze command. The Time Registers start at offset 0xFC. They contain packed BCD data, except for the Status bits. Table 2-6 shows the location of the Time Registers.

GPS position consists of latitude and longitude (in degrees, minutes, and seconds with north, south, east, and west indicators) and elevation (in meters above or below sea level). The position information actually defines the location of the GPS antenna. The position information is updated every 16 seconds.

The Position Registers start at offset 0x108. They contain packed BCD data except for the north, south, east, west, and sign indicators, which are ASCII byte values. Table 2-6 shows the location of data in the Position Registers.

TABLE 2-6
TIME/POSITION FREEZE REGISTERS

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Time	Tens microseconds (BCD)				Unit microseconds (BCD)				0xFC	0xFC
Time	Unit milliseconds (BCD)				Hundreds microseconds (BCD)				0xFD	
Time	Hardware Status Register[1]				Not Defined				0xFE	
Time	Not Defined				Not Defined				0xFF	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x100	0x100
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x101	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x102	
Time	Tens hours (BCD)				Unit hours (BCD)				0x103	
Time	Tens days (BCD)				Unit days (BCD)				0x104	0x104
Time	Status[2]				Hundreds days (BCD)				0x105	
Time	Tens years (BCD)				Unit years (BCD)				0x106	
Time	Thousands years (BCD)				Hundreds years (BCD)				0x107	
Latitude	Tens degrees (BCD)				Unit degrees (BCD)				0x108	0x108
Latitude	0				Hundreds degrees (BCD)				0x109	
Latitude	Tens minutes (BCD)				Unit minutes (BCD)				0x10A	
Latitude	North/South Byte -- ASCII 'N' (0x4E) / ASCII 'S' (0x53)								0x10B	
Latitude	0				tenths seconds (BCD)				0x10C	0x10C
Latitude	Tens seconds (BCD)				Unit seconds (BCD)				0x10D	
Longitude	Tens degrees (BCD)				Unit degrees (BCD)				0x10E	
Longitude	0				Hundreds degrees (BCD)				0x10F	
Longitude	Tens minutes (BCD)				Unit minutes (BCD)				0x110	0x110
Longitude	Direction E/W Byte -- ASCII 'E' (0x45) / ASCII 'W' (0x57)								0x111	
Longitude	0				tenths seconds (BCD)				0x112	
Longitude	Tens seconds (BCD)				Unit seconds (BCD)				0x113	
Elevation	Tens kilometers (BCD)				Unit kilometers				0x114	0x114
Elevation	Sign Byte-- ASCII '-' (0x2D) / ASCII '+' (0x2B)								0x115	
Elevation	Unit meters				tenths meters				0x116	
Elevation	Hundreds meters				Tens meters				0x117	

Note 1. See Section 2.3.11
Note 2. Status Bits:
B6 - 1 Indicates Phase Locked to Input Code or External 1 PPS.
B5 - 1 Indicates Time Code or External 1 PPS Input Valid.
B4 - 1 Indicates Locked to GPS.

2.3.5.4 PRESET POSITION

The eight locations shown in the table below are used to preset the GPS position. First, write the position into the Preset Time/Position Registers. Table 2-7 shows the data and offset of each register. Write packed BCD data to each register. Then set the Preset Position Ready bit of the Configuration Register. This bit will automatically clear once the position is loaded.

Presetting an initial position will speed up acquisition time by a minute or two.

TABLE 2-7
PRESET TIME/POSITION REGISTERS

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Time	0				0				0x158	0x158
Time	Units milliseconds (BCD)				0				0x159	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x15A	
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x15B	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x15C	0x15C
Time	Tens hours (BCD)				Unit hours (BCD)				0x15D	
Time	Tens days (BCD)				Unit days (BCD)				0x15E	
Time	0				Hundreds days (BCD)				0x15F	
Time	Tens years (BCD)				Unit years (BCD)				0x160	0x160
Time	Thousands years (BCD)				Hundreds years (BCD)				0x161	
Time	0				0				0x162	
Time	0				0				0x163	
Latitude	Tens degrees (BCD)				Unit degrees (BCD)				0x164	0x164
Latitude	0				Hundreds degrees (BCD)				0x165	
Latitude	Tens minutes (BCD)				Unit minutes (BCD)				0x166	
Latitude	North/South Byte -- ASCII ‘N’ (0x4E) / ASCII ‘S’ (0x53)								0x167	
Latitude	0				tenths seconds (BCD)				0x168	0x168
Latitude	Tens seconds (BCD)				Unit seconds (BCD)				0x169	
Longitude	Tens degrees (BCD)				Unit degrees (BCD)				0x16A	
Longitude	0				Hundreds degrees (BCD)				0x16B	
Longitude	Tens minutes (BCD)				Unit minutes (BCD)				0x16C	0x16C
Longitude	East/West Byte -- ASCII ‘E’ (0x45) / ASCII ‘W’ (0x57)								0x16D	
Longitude	0				tenths seconds (BCD)				0x16E	
Longitude	Tens seconds (BCD)				Unit seconds (BCD)				0x16F	
Elevation	Tens kilometers (BCD)				Unit kilometers				0x170	0x170
Elevation	Sign Byte-- ASCII ‘-’ (0x2D) / ASCII ‘+’ (0x2B)								0x171	
Elevation	Unit meters				tenths meters				0x172	
Elevation	Hundreds meters				Tens meters				0x173	

2.3.5.5 SIGNAL LEVELS

Signal levels (are provided for up to six satellites in bank 5). Both the PRN (satellite ID) and signal level are in packed BCD. When the flag byte is set it indicates that either the information is not available or it is being updated. The signal level information is updated approximately every 10 seconds. Signal levels are normally positive. If it is zero then that satellite has not yet been acquired or is not currently in lock. The signal level is a measure of the signal strength after correlation or de-spreading. A good signal level magnitude is eight or more. Table 2-8 shows the data.

TABLE 2-8
SIGNAL LEVELS

DESCR	DATA								OFFSET	
	B7	B6	B5	B4	B3	B2	B1	B0	BYTE	DWORD
PRN #1	Tens (BCD)				Units (BCD)				0x198	0x198
PRN #1	0				0				0x199	
Level #1	tenths (BCD)				hundredths (BCD)				0x19A	
Level #1	Tens (BCD)				Hundreds (BCD)				0x19B	
PRN #2	Tens (BCD)				Units (BCD)				0x19C	0x19C
PRN #2	0				0				0x19D	
Level #2	tenths (BCD)				hundredths (BCD)				0x19E	
Level #2	Tens (BCD)				Hundreds (BCD)				0x19F	
PRN #3	Tens (BCD)				Units (BCD)				0x1A0	0x1A0
PRN #3	0				0				0x1A1	
Level #3	tenths (BCD)				hundredths (BCD)				0x1A2	
Level #3	Tens (BCD)				Hundreds (BCD)				0x1A3	
PRN #4	Tens (BCD)				Units (BCD)				0x1A4	0x1A4
PRN #4	0				0				0x1A5	
Level #4	tenths (BCD)				Hundredths (BCD)				0x1A6	
Level #4	Tens (BCD)				Hundreds (BCD)				0x1A7	
PRN #5	Tens (BCD)				Units (BCD)				0x1A8	0x1A8
PRN #5	0				0				0x1A9	
Level #5	tenths (BCD)				Hundredths (BCD)				0x1AA	
Level #5	Tens (BCD)				Hundreds (BCD)				0x1AB	
PRN #6	Tens (BCD)				Units (BCD)				0x1AC	0x1AC
PRN #6	0				0				0x1AD	
Level #6	tenths (BCD)				Hundredths (BCD)				0x1AE	
Level #6	Tens (BCD)				Hundreds (BCD)				0x1AF	
Flag	Flag								0x1B0	0x1B0
Flag	Not Defined				Not Defined				0x1B1	
Flag	Not Defined				Not Defined				0x1B2	
Flag	Not Defined				Not Defined				0x1B3	

2.3.6 EXTERNAL EVENT

To record the time of an event, input a pulse at pin 1 of the 9-pin connector which will freeze the time in the External Event Time Registers. A flag in the Hardware Status Register will set when the External Event Time is available (this may take up to 2 ms) (Section 2.3.11). The External Event Time Registers will contain the time of the first event, accurate to within 3 μs. To clear the flag and enable the unit to capture another event, write to the Hardware Control Register (Section 2.3.12). The location of the registers and the packed BCD data are shown in Table 2-9. The external event can generate an interrupt (Section 2.3.12).

The External Event Logic can process events at a maximum rate of 100 pulses per second. The pulses need to be at least 3 ms apart. When IRIG-A is the synchronized generator reference, do not use the external event capability. It may cause an error in the time code valid status.

TABLE 2-9
EXTERNAL EVENT TIME REGISTERS

DESCR	DATA B7	B6	B5	B4	B3	B2	B1	B0	OFFSET BYTE	OFFSET DWORD
Time	Tens microseconds (BCD)				Unit microseconds (BCD)				0x174	0x174
Time	Unit milliseconds (BCD)				Hundreds microseconds (BCD)				0x175	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x176	
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x177	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x178	0x178
Time	Tens hours (BCD)				Unit hours (BCD)				0x179	
Time	Tens days (BCD)				Unit days (BCD)				0x17A	
Time	Status[1]				Hundreds days (BCD)				0x17B	
Time	Tens years (BCD)				Unit years (BCD)				0x17C	0x17C
Time	Thousands years (BCD)				Hundreds years (BCD)				ox17D	
Time	Not Defined				Not Defined				0x17E	
Time	Not Defined				Not Defined				0x17F	

Note 1. Status Bits:
B7 - Not Defined. B5 - 1 indicates Time Code Input Valid.
B6 - 1 indicates Phase Locked to Input Code. B4 - 1 indicates Locked to GPS.

2.3.7 RATE GENERATOR

The Rate Generator can output a signal at pin 7 of the 9-pin connector with one of five fixed rates. The Rate Generator signal is synchronous with the board timing and the rising edge is on time.

Write a BCD value to the upper nibble of the Configuration Rate Register to select the rate of the output signal.

The Rate Generator signal can trigger a bus interrupt (Section 2.3.12). The Rate bit of the Hardware Status Register also indicates when a Rate pulse has occurred (Section 2.3.11).

TABLE 2-10
CONFIGURATION RATE REGISTER

BCD VALUE	RATE
0	Disabled
1	10 KPPS
2	1 KPPS
3	100 PPS
4	10 PPS
5	1 PPS

2.3.8 TIME COMPARE

The user may program the Time Compare output to produce a pulse at a preset time. When the Generator time is equal to the value in the Time Compare registers, a pulse will output at the 9-pin connector pin 6. The rising edge of this pulse is on-time. The pulse width depends on the programmed microseconds and can be from approximately 1 to 3 milliseconds wide. If the programmed microseconds are zero, then the pulse

width will be 2ms. This pulse may be used to generate an interrupt (Section 2.3.12). The Time-Comp bit of the Hardware Status Register indicates when a Time Compare has occurred.

Load the desired time of the time compare in the Time Compare Registers. Table 2-11 defines the locations and data for the Time Compare Registers. Data is packed BCD.

TABLE 2-11
TIME COMPARE REGISTERS

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Time	Tens microseconds (BCD)				Unit microseconds (BCD)				0x138	0x138
Time	Unit milliseconds (BCD)				Hundreds microseconds (BCD)				0x139	
Time	Hundreds milliseconds (BCD)				Tens milliseconds (BCD)				0x13A	
Time	Tens seconds (BCD)				Unit seconds (BCD)				0x13B	
Time	Tens minutes (BCD)				Unit minutes (BCD)				0x13C	0x13C
Time	Tens hours (BCD)				Unit hours (BCD)				0x13D	
Time	Tens days (BCD)				Unit days (BCD)				0x13E	
Time	Mask[1]				Hundreds days (BCD)				0x13F	

Note1. Mask B7:3 Value:

0x0 Compare Hday through us.	0x6 Compare Umin through us.
0x1 Compare Tday through us.	0x7 Compare Tsec through us.
0x2 Compare Uday through us.	0x8 Compare Usec through us.
0x3 Compare Thr through us.	0x9 Compare Hms through us.
0x4 Compare Uhr through us.	0xA Compare Tms through us.
0x5 Compare Tmin through us.	0xB Compare Ums through us.

The mask nibble is a hexadecimal number between 0x0 and 0xB. The mask limits the data used in the time compare operation. For example, if the mask value is 0x0, all data (hundreds of days through microseconds) are compared. If the mask value is a 0x1, then hundreds of days is ignored.

The mask can be used to output pulses at regular time intervals. For example, a mask value of 0xB causes a comparison of the microseconds through milliseconds data resulting in a pulse every ten milliseconds at the precise microsecond programmed.

2.3.9 OSCILLATOR DISCIPLINE

The PCI-SG drives the on-board Temperature Compensated Crystal Oscillator (TCXO) control voltage to remove frequency difference relative to the external reference.

The accumulative phase error due to the frequency error of the oscillator drives the voltage control circuitry. If the reference is lost, oscillator discipline ceases. The time will drift at a rate dependent on the current oscillator frequency error. This error is affected by changes in temperature. See Section 1.8 for specifications.

2.3.10 DIAGNOSTIC REGISTER

The Diagnostic Register at 0x11C contains the results of a diagnostic test that is done at power-up and during normal operation. The bits in the least significant byte represent a potential error. If the bit is set, that error has occurred. Table 2-12 defines the meaning of each bit.

The oscillator status, available in the Diagnostic Register at offset 0x11E, contains a 16-bit value representing the current output of the frequency-control digital-to-analog converter (DAC). The DAC output controls the frequency of the crystal oscillator used as the time base for the PCI-SG. This output will range from 0x0000 to 0xFFFF hexadecimal. This value may vary from its midrange value significantly depending on the accuracy, stability of the reference frequency, the ambient temperature and oscillator aging.

TABLE 2-12
DIAGNOSTIC REGISTER

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Diag	Error Status[1]								0x11C	0x11C
Diag	Not Defined								0x11D	
Diag	Oscillator Status[2]								0x11E	
Diag	Oscillator Status[2]								0x11F	

Note 1. Status Bits:
B7:4 Reserved.
B3 - 1 indicates hardware failure.
B2 - 1 indicates DAC setting near limit.
B1 - 1 indicates on-board RAM failure..
B0 - 1 indicates Processor Clock failure.

Note 2. Oscillator Status
16-Bits - Current setting of Frequency Control DAC.

2.3.11 HARDWARE STATUS REGISTER

The Hardware Status Register is at offset 0xFE. It shows the status of the External Event, Time-Compare, and Rate flags. These flags are always available as status and can be un-masked, via the Hardware Control Register, to generate interrupts. (If polling these flags, do so at a period of 150 microseconds or more. Accessing the card faster than this may prevent the on-board processor from updating the dual-port ram.) The flags are cleared via the Hardware Control Register. Other bits indicate antenna fault status. Table 2-13 defines the meaning of each bit in the Hardware Status Register.

TABLE 2-13
HARDWARE STATUS REGISTER

DESCR	DATA B7	B6	B5	B4	B3	B2	B1	B0	OFFSET BYTE	OFFSET DWORD
Status	Not Defined				Not Defined				0xFC	0xFC
Status	Not Defined				Not Defined				0xFD	
Status	Not Defined Status[1]								0xFE	
Status	Not Defined				Not Defined				0xFF	

Note 1. Status Bits:

B7 - Not Defined.
B6 - Not Defined.
B5 - 0 indicates Antenna shorted.
B4 - 0 indicates Antenna open.
B3 - Not Defined.
B2 - 1 indicates Rate Generator Pulse Occurred.
B1 - 1 indicates Time Compare Pulse Occurred.
B0 - 1 indicates External Event Occurred.

2.3.12 HARDWARE CONTROL REGISTER

Select PCI interrupt sources via the Hardware Control Register located at offset 0xF8.

Any combination of the sources in Table 2-14 may be selected. The External Event, Time-Compare, and Rate flags are always available in the Hardware Status Register and can be un-masked, via bits 3, 4, and 5 to generate interrupts. They are cleared via bits 0, 1, and 2 (writing a 1 to bits 0 through 2 generates a 1-cycle clear pulse). In addition to this register, you may also need to program the INTCSR register at offset 0x4C in the PLX9050 chip. Refer to Section 2.3.16.

TABLE 2-14
HARDWARE CONTROL REGISTER

DESCR	DATA B7	B6	B5	B4	B3	B2	B1	B0	OFFSET BYTE	OFFSET DWORD
Hdwe Cntl	Control[1]								0xF8	0xF8
Hdwe Cntl	Reserved - Always 0								0xF9	
Hdwe Cntl	Reserved - Always 0								0xFA	
Hdwe Cntl	Reserved - Always 0								0xFB	

Note 1. Control Bits:

B7 Reserved.
0 - Always

B6 Reserved.
0 - Always

B5 Rate Generator Interrupt Mask:
0 - Masked.
1 - Not Masked.

B4 Time Compare Interrupt Mask:
0 - Masked.
1 - Not Masked.

B3 External Interrupt Mask:
0 - Masked.
1 - Not Masked.

B2 Rate Generator Status Flag Clear:
0 - No Effect
1 - Clear (Generates 1-cycle pulse).

B1 Time Compare Status Flag Clear:
0 - No Effect.
1 - Clear (Generates 1-cycle pulse).

B0 External Event Status Flag:
0 - No Effect.
1 - Clear (Generates 1-cycle pulse).

2.3.13 CONFIGURATION REGISTER

The following is a summary of the Configuration Register located at offset 0x118. Table 2-15 shows the bit definitions.

TABLE 2-15
CONFIGURATION REGISTER

DATA									OFFSET	
DESCR	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	**BYTE**	**DWORD**
Config	Control[1]								0x118	0x118
Config	Code[2]								0x119	
Config	Rate - Reserved				Rate - Reserved				0x11A	
Config	Rate - Flag[3]				Rate - Reserved				0x11B	

Note 1. Control Bits:

B7 Preset Position Ready
- 0 - Preset Position Ready
- 1 - GPS Position has been preset

B6 Select 1 PPS Reference
- 0 - Disabled
- 1 - Enabled

B5 Select GPS Reference
- 0 - Disabled
- 1 - Enabled

B4 Select Time Code Reference
- 0 - Disabled
- 1 - Enabled

B3 Generator Stop
- 0 - Generator Run
- 1 - Generator Stop

B2 Preset Time Ready
- 0 - Preset Time Ready
- 1 - Generator Time has been preset

B1 DST
- 0 - Disabled
- 1 - Enabled

B0 Mode Select
- 0 - Generator Mode
- 1 - Synchronized Generator Mode

Note 2. Code Bits:

B7:0 = AM
- 1 = DC

B6:4 Reserved
- 0x0 - Always
- 0x1-F - Reserved

B3:0 Input Code Select
- 0x0 - IRIG B
- 0x1 - IRIG A
- 0x2-F - Reserved

Note3. Flag B7:4 Flag:
- 0x0 Disabled
- 0x1 10K PPS
- 0x2 1K PPS
- 0x3 100 PPS
- 0x4 10 PPS
- 0x5 1 PPS

2.3.13.1 CONTROL BYTE

Mode Select. Set bit 0 of the Control byte to select Synchronized Generator mode. Clear bit 0 to select Generator mode.

DST. Set bit 1 to enable automatic DST transitions in GPS Synchronized Generator Mode.

Preset Time Ready. Bit 2 controls the presetting of the Generator time. When this bit is set the time in the Time Preset Registers will be transferred to the Generator time. This bit will self-clear after the preset has completed. Valid only in generator mode.

Generator Stop. Set bit 3 to stop the Generator. Clear bit 3 to start the Generator. This has no effect when in Synchronized Generator mode.

Reference Select. Set bits 4, 5, and 6 of the Control byte to select the Synchronized Generator Input Time Reference. Use the specified bit pattern to select between Time Code, GPS, or 1 PPS via the External Event input. These bits are mutually exclusive. If more than one is set, results are undefined.

Preset Position Ready. Bit 7 controls presetting the GPS Module position. When this bit is set, the position in the Position Preset Registers will be transferred to the GPS Module. This bit will self-clear after the preset has completed.

2.3.13.2 CODE BYTE

Input Code Select. Set bit 7 to select DC as Synchronized Generator Time Code Reference. Clear bit 7 to select AM code. Set bits 3 through 0 to select between IRIG-A and IRIG-B (see Section 2.3.4.1).

2.3.13.3 RATE BYTES

Flag. Set the flag bits 7:4 to select the rate for the Rate Generator Output. Select fixed rates from 1 PPS to 10K PPS (see Section 2.3.7).

2.3.14 MEMORY MAP

Table 2-16 defines the PCI-SG memory map. All locations are described by the offset from the PCI Base Address Register 3.

TABLE 2-16
MEMORY MAP

ADRS OFFSET		CONTENTS	
DWORD	**BYTE**	**DESCRIPTION**	**NOTES**
0x00	All	Reserved	
THRU	All	Reserved	
0xF7	All	Reserved	
0xF8 {	0xF8	Hardware Control Register	
write {	0xF9	Hardware Control Register - Not Defined	
only {	0xFA	Hardware Control Register - Not Defined	
{	0xFB	Hardware Control Register - Not Defined	
0xFC	0xFC	Freeze Register - Tus Uus (FREEZE command)	
	0xFD	Freeze Register - Ums Hus	
	0xFE	Hardware Status Register	
	0xFF	Freeze Register - Not Defined	
0x100	0x100	Freeze Register - Hms Tms	
	0x101	Freeze Register - Tsec Usec	
	0x102	Freeze Register - Tmin Umin	
	0x103	Freeze Register - Thr Uhr	
0x104	0x104	Freeze Register - Hday Tday	
	0x105	Freeze Register - Status Hday	
	0x106	Freeze Register - Tyr Uyr	
	0x107	Freeze Register - Kyr Hyr	
0x108	0x108	Freeze Register - Latitude Tdeg Udeg	
	0x109	Freeze Register - Latitude 0 Hdeg	
	0x10A	Freeze Register - Latitude Tmin Umin	
	0x10B	Freeze Register - Latitude N/S	

0x10C	0x10C	Freeze Register - Latitude 0 tsec	
	0x10D	Freeze Register - Latitude Tsec Usec	
	0x10E	Freeze Register - Longitude Tdeg Udeg	
	0x10F	Freeze Register - Longitude 0 Hdeg	
0x110	0x110	Freeze Register - Longitude Tmin Umin	
	0x111	Freeze Register - Longitude E/W	
	0x112	Freeze Register - Longitude 0 tsec	
	0x113	Freeze Register - Longitude Tsec Usec	
0x114	0x114	Freeze Register - Tkm Ukm	
	0x115	Freeze Register - Sign	
	0x116	Freeze Register - Um tm	
	0x117	Freeze Register -Hm Tm	
0x118	0x118	Configuration Register - Control	Stored[1]
	0x119	Configuration Register - Code	Stored
	0x11A	Configuration Register - Rate Reserved	Stored
	0x11B	Configuration Register - Rate Flag	Stored
0x11C	0x11C	Diagnostic Register - Error	
	0x11D	Diagnostic Register - Not Defined	
	0x11E	Diagnostic Register - Oscillator Status - Lo	
	0x11F	Diagnostic Register - Oscillator Status - Hi	
0x120	0x120	Local Offset - Tmin Umin	Stored
	0x121	Local Offset - Thr Uhr	Stored
	0x122	Local Offset - Sign	Stored
	0x123	Local Offset - 0	Stored
0x124	0x124	Synchronized Generator Offset - Lo	Stored
	0x125	Synchronized Generator Offset - Hi	Stored
	0x126	Synchronized Generator Offset - 0	Stored
	0x127	Synchronized Generator Offset - 0	Stored
0x128	0x128	Reserved for Future Use	
	0x129	Reserved for Future Use	
	0x12A	Reserved for Future Use	
	0x12B	Reserved for Future Use	
0x12C	0x12C	Configuration Register #2 - Control	
	0x12D	Configuration Register #2 - Reserved	
	0x12E	Configuration Register #2 - Reserved	
	0x12F	Configuration Register #2 - Reserved	
0x130	0x130	Reserved	
	0x131	Reserved	
	0x132	Reserved	
	0x133	Reserved	
0x134	0x134	Reserved	
	0x135	Reserved	
	0x136	Reserved	
	0x137	Reserved	
0x138	0x138	Time Compare - Tus Uus	
	0x139	Time Compare - Ums Hus	
	0x13A	Time Compare - Hms Tms	
	0x13B	Time Compare - Tsec Usec	
0x13C	0x13C	Time Compare -Tmin Umin	
	0x13D	Time Compare -Thr Uhr	
	0x13E	Time Compare -Tday Uday	
	0x13F	Time Compare - Mask Hday	
0x140	0x140	Undefined	
	0x141	Undefined	
	0x142	Undefined	
	0x143	Undefined	
0x144	0x144	Undefined	
	0x145	Undefined	

	0x146	Undefined	
	0x147	Undefined	
0x148	0x148	Undefined	
	0x149	Undefined	
	0x14A	Undefined	
	0x14B	Undefined	
0x14C	0x14C	Undefined	
	0x14D	Undefined	
	0x14E	Undefined	
	0x14F	Undefined	
0x150	0x150	Undefined	
	0x151	Undefined	
	0x152	Undefined	
	0x153	Undefined	
0x154	0x154	Undefined	
	0x155	Undefined	
	0x156	Undefined	
	0x157	Undefined	
0x158	0x158	Preset Time - 0 0	
	0x159	Preset Time - Ums 0	
	0x15A	Preset Time - Hms Tms	
	0x15B	Preset Time - Tsec Usec	
0x15C	0x15C	Preset Time -Tmin Umin	
	0x15D	Preset Time - Thr Uhr	
	0x15E	Preset Time - Tday Uday	
	0x15F	Preset Time - 0 Hday	
0x160	0x160	Preset Time - Tyr Uyr	Stored
	0x161	Preset Time - Kyr Hyr	Stored
	0x162	Preset Time - 0 0	
	0x163	Preset Time - 0 0	
0x164	0x164	Preset Position - Latitude Tdeg Udeg	
	0x165	Preset Position - Latitude 0 Hdeg	
	0x166	Preset Position - Latitude Tmin Umin	
	0x167	Preset Position - Latitude N/S	
0x168	0x168	Preset Position - Latitude 0 tsec	
	0x169	Preset Position - Latitude Tsec Usec	
	0x16A	Preset Position - Longitude Tdeg Udeg	
	0x16B	Preset Position - Longitude 0 Hdeg	
0x16C	0x16C	Preset Position - Longitude Tmin Umin	
	0x16D	Preset Position - Longitude E/W	
	0x16E	Preset Position - Longitude 0 tsec	
	0x16F	Preset Position - Longitude Tsec Usec	
0x170	0x170	Preset Elevation - Tkm Ukm	
	0x171	Preset Elevation - Sign	
	0x172	Preset Elevation - Um tm	
	0x173	Preset Elevation - Hm Tm	
0x174	0x174	External Event - Tus Uus	
	0x175	External Event - Ums Hus	
	0x176	External Event - Hms Tms	
	0x177	External Event - Tsec Usec	
0x178	0x178	External Event - Tmin Umin	
	0x179	External Event - Thr Uhr	
	0x17A	External Event - Tday Uday	
	0x17B	External Event - Status Hday	
0x17C	0x17C	External Event - Tyr Uyr	
	0x17D	External Event - Kyr Hyr	
	0x17E	External Event - Not Defined	
	0x17F	External Event - Not Defined	

0x180	0x180	Undefined	
	0x181	Undefined	
	0x182	Undefined	
	0x183	Undefined	
0x184	0x184	Undefined	
	0x185	Undefined	
	0x186	Undefined	
	0x187	Undefined	
0x188	0x188	Undefined	
	0x189	Undefined	
	0x18A	Undefined	
	0x18B	Undefined	
0x18C	0x18C	Undefined	
	0x18D	Undefined	
	0x18E	Undefined	
	0x18F	Undefined	
0x190	0x190	Undefined	
	0x191	Undefined	
	0x192	Undefined	
	0x193	Undefined	
0x194	0x194	Undefined	
	0x195	Undefined	
	0x196	Undefined	
	0x197	Undefined	
0x198	0x198	Signal Level - #1 PRN Tens Units	
	0x199	Signal Level - #1 PRN 0 0	
	0x19A	Signal Level - Level Tenths Hundredths	
	0x19B	Signal Level - Level Tens Units	
0x19C	0x19C	Signal Level - #2 PRN Tens Units	
	0x19D	Signal Level - #2 PRN 0 0	
	0x19E	Signal Level - Level Tenths Hundredths	
	0x19F	Signal Level - Level Tens Units	
0x1A0	0x1A0	Signal Level - #3 PRN Tens Units	
	0x1A1	Signal Level - #3 PRN 0 0	
	0x1A2	Signal Level - Level Tenths Hundredths	
	0x1A3	Signal Level - Level Tens Units	
0x1A4	0x1A4	Signal Level - #4 PRN Tens Units	
	0x1A5	Signal Level - #4 PRN 0 0	
	0x1A6	Signal Level - Level Tenths Hundredths	
	0x1A7	Signal Level - Level Tens Units	
0x1A8	0x1A8	Signal Level - #5 PRN Tens Units	
	0x1A9	Signal Level - #5 PRN 0 0	
	0x1AA	Signal Level - Level Tenths Hundredths	
	0x1AB	Signal Level - Level Tens Units	
0x1AC	0x1AC	Signal Level - #6 PRN Tens Units	
	0x1AD	Signal Level - #6 PRN 0 0	
	0x1AE	Signal Level - Level Tenths Hundredths	
	0x1AF	Signal Level - Level Tens Units	
0x1B0	0x1B0	Signal Level - Flag	
	0x1B1	Signal Level - Not Defined	
	0x1B2	Signal Level - Not Defined	
	0x1B3	Signal Level - Not Defined	
0x1B4	0x1B4	Reserved for Test	
	0x1B5	Reserved for Test	
	0x1B6	Reserved for Test	
	0x1B7	Reserved for Test	
0x1B8	0x1B8	Reserved	
	0x1B9	Reserved	

	0x1BA	Reserved	
	0x1BB	Reserved	
0x1BC	0x1BC	Reserved	
	0x1BD	Reserved	
	0x1BE	Reserved	
	0x1BF	Reserved	

Note 1. STORED parameters are retained while the PCI-SG power is off.

2.3.15 PCI CONFIGURATION HEADER REGION

The PCI-SG possesses a block of 64 configuration double words reserved for the implementation of its configuration registers. The first 16 double words are predefined by the PCI specification. This area is referred to as the configuration header region. To uniquely identify the PCI-SG the following registers are:

Device ID:	0X9050
Vendor ID:	0x10B5
Subsystem Vendor ID:	0x12DA
Subsystem ID:	0x5900

2.3.16 CompactPCI LOCAL CONFIGURATION REGISTERS

The CompactPCI-SG possesses a block of 32 double word registers reserved for local configuration purposes. This area is referred to as the Local Configuration Registers and is physically mapped both to memory and to I/O addresses at run time. The memory mapped versions' base address is located at 0x10 in the CONFIGURATION HEADER REGION and the base address for the I/O mapped version is at 0x14. Either I/O or memory read or write cycles may be used to access the LCRs. Normally, only one register will ever be accessed by the user, the INTCSR Register at location 0x4C.

CAUTION: Writing to other registers in this region runs the risk of locking up your computer or causing other unusual symptoms, requiring a reboot to recover.

Writing a value of xxxxxx48h to this register will enable the PLX9050 chip to pass along interrupts from the card if they are enabled elsewhere. The card is normally shipped with this value preconfigured, however, it is possible that this value has been changed from the default and you will need to know how to set it back. Note that the value xxxxxx08h will disable all interrupts.

SECTION THREE

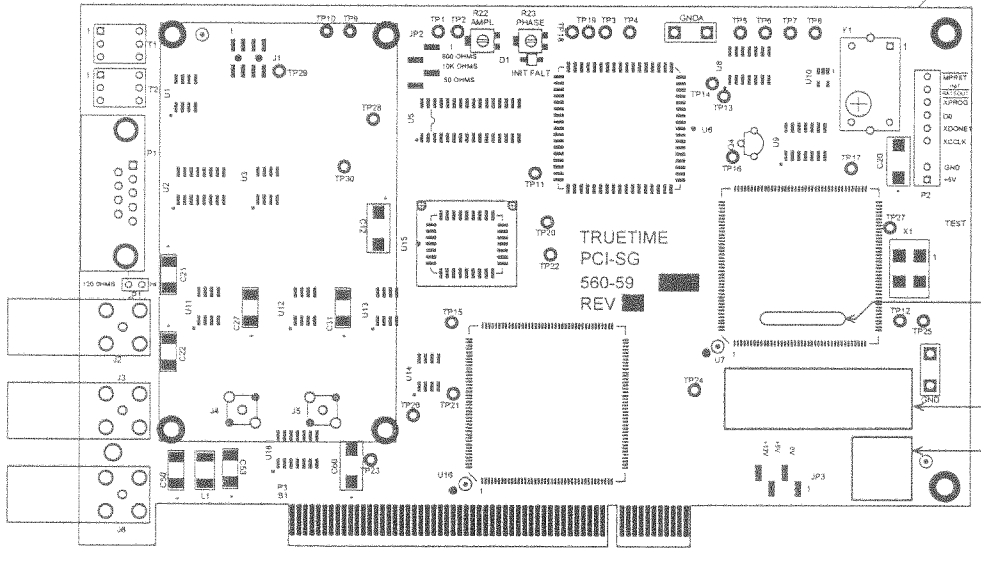
DRAWINGS

NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY REVISION LEVEL.
2. RESISTORS ARE IN OHMS AND CAPACITORS ARE IN MICRO FARADS.
3. ASSEMBLE PER ASSEMBLY REQUIRMENTS DOCUMENT 421-11.
4. DO NOT INSTALL: TP1-10, T1,T2, P2,P3, C51, J5,R10,20,48,51,54,65,68-71,73,80,85,94,95,97,98.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
02	DESIGN CHANGE	5/97	
03	ECO1098, ECO1099	6/18/97	
04	CAR# 766	4/22/98	
A	ECO# 1156	06/26/98	
B	ECO#1220	04/20/99	
C	ECO#1221	04/21/99	
D	ECO#1227	06/16/99	
E	CAR #3652 & 3677	10/07/99	mgm 10/7/99

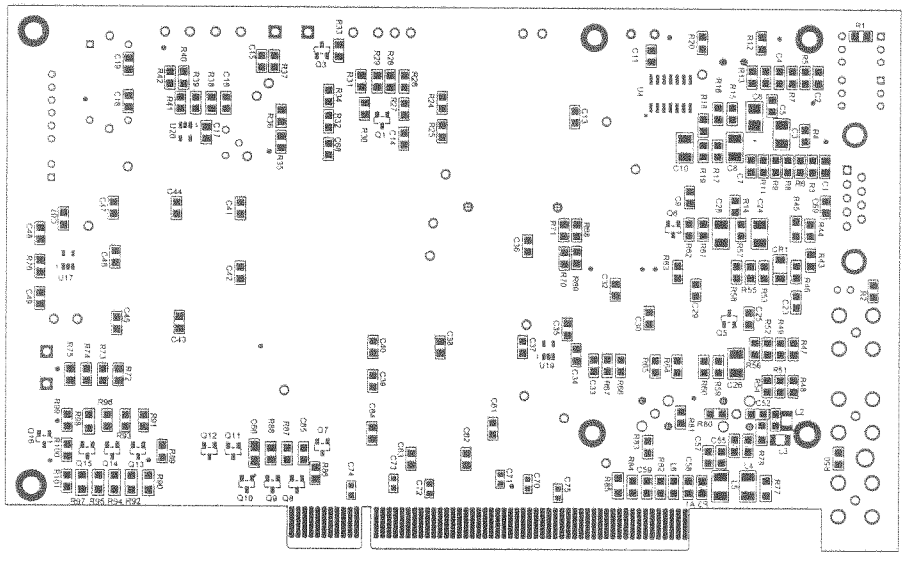


TOP SIDE

CONTRACT NO.		
APPROVALS	DATE	
DRAWN BY S.B.K.	6-18-97	
CHECKED		
APPROVED	mgm 10/7/99	
NEXT ASSY		

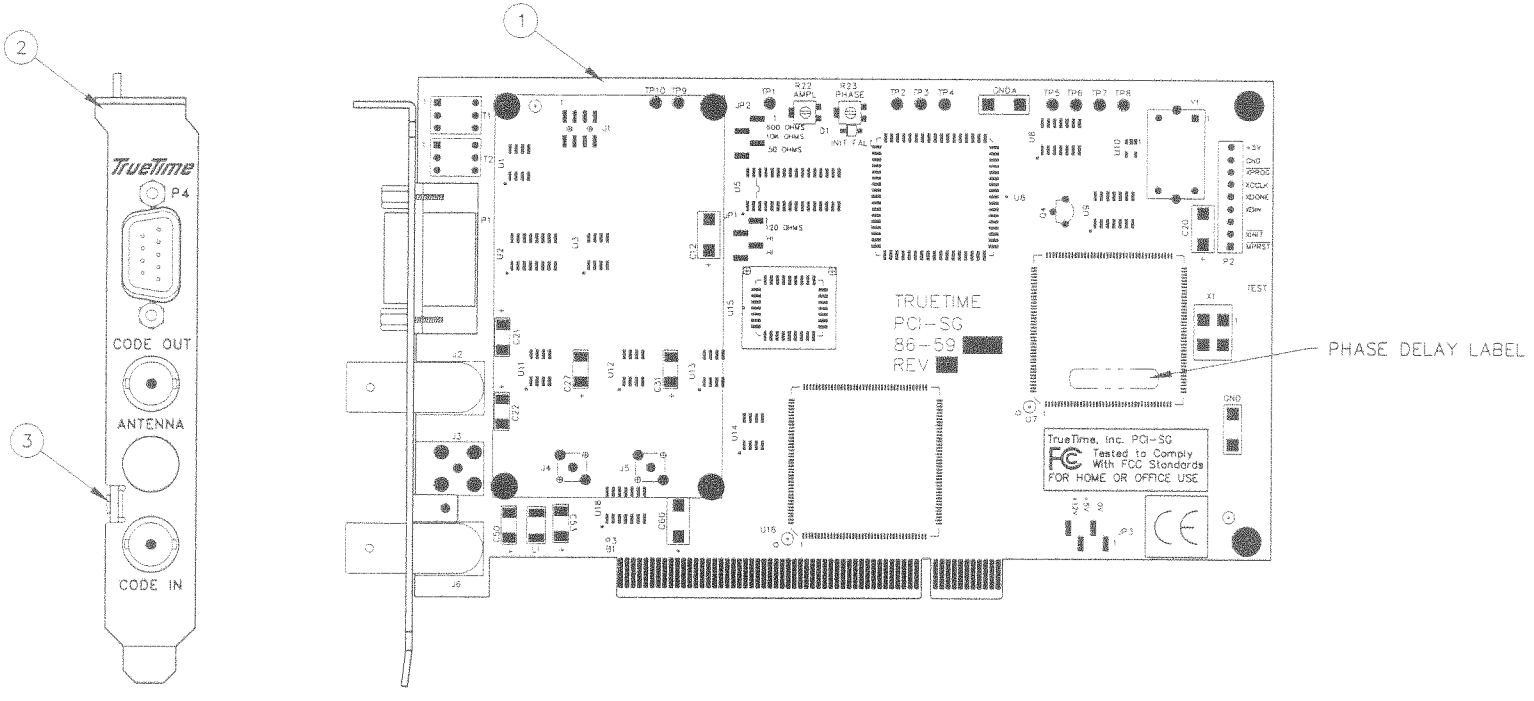
TrueTime, Inc.
Santa Rosa, California

Title	PCI-SG ASSY DRAWING	
Size B	Number 560-5900	Rev E
Date 10/07/99		Drawn By S.B.K.
Filename 2900A.PCB		Sheet 1 of 10



BOTTOM SIDE

TrueTime, Inc.		
Santa Rosa, California		
Title	PCI-SG ASSY DRAWING	
Size B	Number 560-5900	Rev E
Date 10/07/99		Drawn By S.B.K.
Filename 2900A.PCB		Sheet 2 of 10



TrueTime®
"Where Customer Satisfaction is our Highest Priority"
2835 Duke Ct. Santa Rosa, CA 95407

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		560-5900	E

SCALE NONE | SHEET 3 OF 10

FILENAME: \560\5900
DATE: 10-07-99

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5900	ASSY PCB PCI (BASIC)	MADE FROM 560-2900				EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		MSM 10/07/99
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV E (10-07-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		560-5900 REV E
0000-REV	PCB REV LEVEL HERE >>>>		000000		1.0000	EA		560-2900 REV A
002S-000	RES 0805 0 OHM	CAL-CHIP RM10J000CT (NAV)	000000		5.0000	EA		R1,2,12,50,60
002S-130	RES 1206 13 OHM 1% 1/4W	CAL-CHIP RM12F13ROCT(NAV)	000000		2.0000	EA		R90,92
002S-510	RES 1206 51 OHM 5% 1/4W	CAL-CHIP RM12J510CT (NAV)	000000		3.0000	EA		R45,77,78
008S-1002	RES 0805 10K OHM 1% 1/8W	CAL-CHIP RM10F1002CT(NAV)	000000		14.0000	EA		
	R8,26,28,29,31,32,34-37,39,41,43,101							
008S-102	RES 0805 1K OHM 1% 1/8W	CAL-CHIP RM10F1001CT(NAV)	000000		2.0000	EA		R5,84
008S-104	RES 0805 100K OHM 1% 1/8W	CAL-CHIP RM10F1003CT(NAV)	000000		3.0000	EA		R42,82,83
008S-105	RES 0805 1M 5% 1/8W	CAL-CHIP RM10J105CT (NAV)	000000		1.0000	EA		R76
008S-1152	RES 0805 11.5KOHM 1% 1/8W	CAL-CHIP RM10F1152CT(NAV)	000000		3.0000	EA		R18,19,57
008S-121	RES 0805 120 OHM 5% 1/8W	CAL-CHIP RM10J121CT (NAV)	000000		1.0000	EA		R3
008S-1211	RES 0805 1.21K 1% 1/8W	CAL-CHIP RM10F1211CT(NAV)	000000		1.0000	EA		R62
008S-152	RES 0805 1.5K OHM 5% 1/8W	CAL-CHIP RM10J152CT (NAV)	000000		1.0000	EA		R53
008S-154	RES 0805 150K OHM 5% 1/8W	CAL-CHIP RM10J154CT (NAV)	000000		2.0000	EA		R52,67
008S-2003	RES 0805 200K OHM 1% 1/8W	CAL-CHIP RM10F2003CT(NAV)	000000		2.0000	EA		R13,38
008S-201	RES 0805 200 OHM 5% 1/8W	CAL-CHIP RM10J201CT (NAV)	000000		1.0000	EA		R96
008S-222	RES 0805 2.2K OHM 5% 1/8W	CAL-CHIP RM10J222CT (NAV)	000000		1.0000	EA		R9
008S-223	RES 0805 22K OHM 5% 1/8W	CAL-CHIP RM10J223CT (NAV)	000000		5.0000	EA		R7,55,56,59,93
008S-225	RES 0805 2.2M OHM 5% 1/8W	CAL-CHIP RM10J225CT (NAV)	000000		1.0000	EA		R46
008S-302	RES 0805 3K OHM 5% 1/8W	CAL-CHIP RM10J302CT (NAV)	000000		1.0000	EA		R64
008S-332	RES 0805 3.3K OHM 5% 1/8W	CAL-CHIP RM10J332CT (NAV)	000000		2.0000	EA		R11,58
008S-391	RES 0805 392 OHM 1% 1/8W	CAL-CHIP RM10F3920CT(NAV)	000000		1.0000	EA		R47
008S-471	RES 0805 470 OHM 5% 1/8W	CAL-CHIP RM10J471CT (NAV)	000000		5.0000	EA		R15,16,40,79,81
008S-472	RES 0805 4.7K OHM 5% 1/8W	CAL-CHIP RM10J472CT (NAV)	000000		17.0000	EA		
	R4,6,14,24,25,27,30,33,61,63,66,72,74,75,88,89,99							
008S-473	RES 0805 47K OHM 5% 1/8W	CAL-CHIP RM10J473CT (NAV)	000000		3.0000	EA		R86,91,100
008S-561	RES 0805 560 OHM 5% 1/8W	CAL-CHIP RM10J561CT (NAV)	000000		1.0000	EA		R87
008S-6191	RES 0805 6.19K 1% 1/10W	CAL-CHIP RM10F6191CT(NAV)	000000		1.0000	EA		R17
008S-621	RES 0805 620 OHM 5% 1/8W	CAL-CHIP RM10J621CT (NAV)	000000		1.0000	EA		R44
008S-753	RES 0805 75K OHM 5% 1/8W	CAL-CHIP RM10J753CT (NAV)	000000		1.0000	EA		R49
019S-001	POT, SNGL TURN SEALED 5K	BOURNS 3314G-1-502E (SMD)	000000		2.0000	EA		R22,23
036S-104	CAP,CHIP .1UF 25V (0603)	ROHM MCH182F104ZK	000000		6.0000	EA		C70-75
036S-NP0120	CAP 12PF NPO 100V 0805 5%	NIC NMC0805NP0120J100TR	000000		1.0000	EA		C54
036S-NP0200	CAP 20PF NPO 100V 0805 5%	NIC NMC0805NP0200J100TR	000000		2.0000	EA		C48,49
036S-NP0220	CAP 22PF NPO 100V 0805 5%	NIC NMC0805NP0220J100TR	000000		1.0000	EA		C52
036S-NP0270	CAP 27PF NPO 100V 0805	NIC NMC0805NP0270J100TR	000000		1.0000	EA		C55
036S-NP0471	CAP 470PF NPO 100V 0805	NMC0805NP0471J100TR (NAV)	000000		1.0000	EA		C58
036S-NP0472	CAP 4.7NF NPO 100V 1210	NMC1210NP0472J100TR (NAV)	000000		2.0000	EA		C10,24
036S-X7R103	CAP .01UF X7R 50V 0805	NIC NMC0805X7R103K50TR	000000		4.0000	EA		C33,56,59,65
036S-X7R104-50	CAP .1UF X7R 50V 0805 10%	NIC NMC0805X7R104K50TR	000000		41.0000	EA		

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

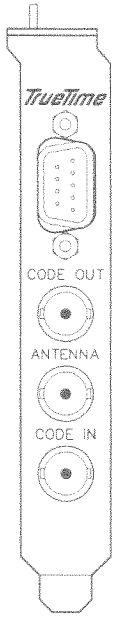
PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
	C1,2,4,5,7,9,11,13-19,23,25,29,30,32,34-47,57,61-64,67-69							
036S-X7R334	CAP .33UF X7R 25V1210 10%	NIC NMC1210X7R334K25TR	000000		2.0000	EA		C3,26
036S-X7R473	CAP 47NF X7R 100V1210 10%	NMC1210X7R473K100TR (NAV)	000000		2.0000	EA		C8,28
037S-105	CAP 1UF 16V 3216	NIC NTC-T105K16TRA	000000		1.0000	EA		C66
037S-106-TL	CAP TANT 10UF 16V SIZE C	PANASONIC ECS-H1CC106R	000000		6.0000	EA		C21,22,27,31,50,53
037S-225	CAP 2.2UF 16V 3528	NIC NTC-T225K16TRB (NAV)	000000		1.0000	EA		C6
037S-686	CAP 68UF 6.3V 7343	NTC-T686K10TRD-BOM NAV	000000		3.0000	EA		C12,20,60
045S-.018UH	INDUCTOR .018UH 1008	NIC NIN-NC18NMTR (NAV)	000000		2.0000	EA		L2,3
045S-27UH	INDUCTOR, HICURRENT, 27UH	TDK NLC1812-270K-T	000000		1.0000	EA		L1
045S-3.3UH	INDUCTOR 3.3UH 1210	NIC NIN-FA3R3KTR	000000		1.0000	EA		L6
045S-56UH	INDUCTOR 56UH 1210	NIC NIN-FA560KTR (NAV)	000000		1.0000	EA		L5
045S-8.2UH	INDUCTOR 8.2UH 1210	NIC NIN-FA8R2KTR	000000		1.0000	EA		L4
057S-4148	DIODE 1N4148	ROHM RLS4148TR	000000		1.0000	EA		CR1
058S-001	LED RED X SML W RES SFMT	HP HLMP-6600-G0012	000000		1.0000	EA		D1
059S-20000	XTAL 20.000 MHZ	MPC SM-65N1B2E-20.000MHZ	000000		1.0000	EA		X1
174S-XC4006E-4	XILINX FPGA XC4006E	XC4006E-4PQ160C	000000		1.0000	EA		U7
175S-2N2907A	TRANSISTOR 2N2907A SOT-23	MOTOROLA MMBT2907AL	000000		9.0000	EA		Q1,7-9,10-12,14,15
175S-3904	XSISTOR,SMALL SIG SOT23	MOTOROLA MMBT3904-LT1	000000		3.0000	EA		Q3,13,16
175S-J177	TRANSISTOR J177 SOT-23	MOTOROLA MMBFJ177L	000000		2.0000	EA		Q5,6
176-34064	UNDER VOLT.SENSING CKT	MOTOROLA MC34064P5	000000		1.0000	EA		Q4
176-68HC11F1	IC, CPU	MOTOROLA MC68HC11F1CFN3	000000		1.0000	EA		U6
176S-29C512-12	FLASH EPROM 64KX8 32PLCC	ATMEL AT29C512-12JC	000000		1.0000	EA		U15
176S-93CS46M	SERIAL EEPROM 1024 BITS	NATL NM93CS46M8(8-P SO)	000000		1.0000	EA		U14
176S-DS8923AM	DS8923AM DIFF DVR/XCVR	NATL DS8923AM (16SO/0.15)	000000		1.0000	EA		U2
176S-LM311M	VOLTAGE COMPARATOR	NATL LM311M (8SOIC)	000000		2.0000	EA		U12,13
176S-MCM6206	MCM6206 32KX8 STATIC RAM	ALLIANCE AS7C256-12JC NAV	000000		1.0000	EA		U5
176S-PCI9050	IC,PCI BUS INTERFACE	PLX PCI9050	000000		1.0000	EA		U16
176S-TL082	J-FET INPUT OP AMP (8SO)	TI TL082BCD	000000		3.0000	EA		U1,3,11
178S-74HC00	74HC00 (14SO)	RCA CD74HC00M	000000		1.0000	EA		U8
178S-74HC04	74HC04 (14SO)	RCA CD74HC04M (NAV)	000000		1.0000	EA		U4
178S-74HC74	74HC74 (14SO)	MOTOROLA MC74HC74D	000000		1.0000	EA		U9
178S-74HCU04	74HCU04 (14SO)	RCA CD74HCU04M	000000		1.0000	EA		U18
178S-NC7SU04	SINGLE INVERTER NC7SU04	NATL NC7SU04M5 (SOT23-5)	000000		4.0000	EA		U10,17,19,20
185-002	PROGRAMMED PROM (PCI)		000000		1.0000	EA		FOR U15
241-002-002	SCREW FH 2-56 X 1/4 IN.	BUY/USE ONLY 100 DEG.	000000		1.0000	EA		03
273-009	TERMINAL TEST POINT	COMP CORP PJ-201-25	000000		2.0000	EA		GND, GNDA
274-008	PLUG HOLE NY .437 DIA.	TROMPETER HP-437	000000		1.0000	EA		ANTENNA
345-032	OSC VCTCXO 16.368	TOYOCOM TCO-919R-16.368	000000		1.0000	EA		Y1
372-09HOOD	CONN 9-P HOOD FOR 372-09	NORCOMP GPH-09A	000000		1.0000	EA		SHIPPING KIT
372-09P	CONN 9-P D-SUB RT ANG ML	AMP 748879-1 (BOM NAV)	000000		1.0000	EA		P1
372-09S	CONN 9-P D-SUB FM S-CUP	ITT CANNON DE-9S	000000		1.0000	EA		SHIPPING KIT
372-609-003	JACK SOCKET SET OF 2	THOMAS & BETTS 609-003	000000		1.0000	EA		FOR P1
373S-001	TERM STRIP 0.25 IN. 4X1	SAMTEC TSM-104-01-T-SV-P	000000		2.0000	EA		JP2,JP3
375-024	CONN BNC RT ANG JK PC MT	AMP 413631-1	000000		2.0000	EA		J2,J6
379S-032	SOCKET 32-P PLCC	AMP 822274-1	000000		1.0000	EA		FOR U15
400-020	LABEL, EPROM 1/4 X 5/8 IN	BRADY, ECL-107-619	000000		0.0010	BX		

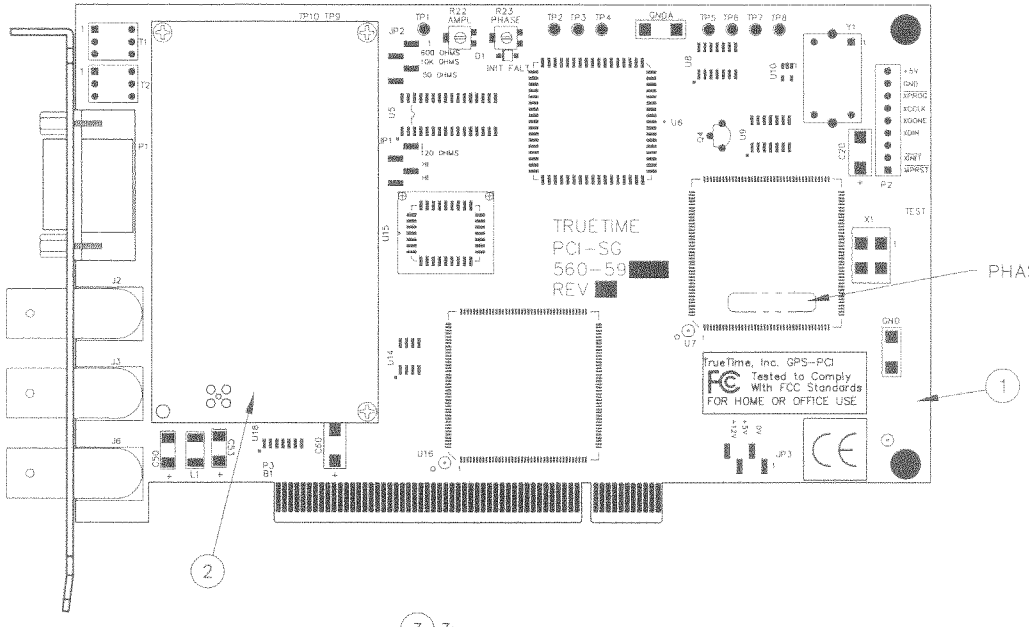
MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

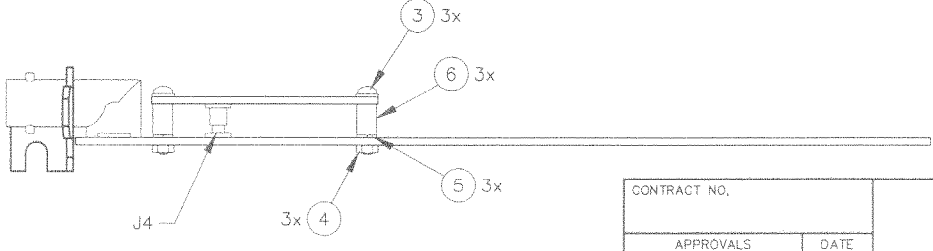
PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
	INSTALL/MARK LABEL FOR THE PHASE DELAY AND AFFIX TO U7 AT FINAL TEST (AT TRUETIME).							
400-078	LABEL,FCC (PCI-SG)	MADE FROM 400-082	000000		1.0000	EA		SEE DWG FOR LOCATION
400-084	LABEL,CE (SMALL)(WHITE)	MADE FROM 400-081	000000		1.0000	EA		SEE DWG FOR LOCATION
401-01-01-34	CONN 36-P HDR SNGL RW W/W	3M 929834-01-36	000000		1.0000	EA		JP1 (CUT TO FIT)
403-000LP	JUMPER FEMALE LOW PROFILE	SAMTEC SNT-100-BK-T	000000		2.0000	EA		JP1,JP2
404S-001	SOCKET STRIP 2MM 4X2(SM)	SAMTEC SMM-104-02-S-D-LC	000000		1.0000	EA		J1
560-1261	PNL,FRONT PCI	GLOBE G6186 (BOM MAV)	000000		1.0000	EA		02
560-2900	PCB PCI	FAB	000000		1.0000	EA		01
560-3170	EPROM PROGRAMMING		000000		1.0000	EA		FOR U14
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		
	DO NOT INSTALL: TP1-30, T1,T2, P2,P3, C51, J5 R10,20,21,48,51,54,65,68-71,73,80,85,94,95,97,98							
OSV560-5900	OUTSIDE LABOR 560-5900	PCA	000000		0	EA		

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 1220	04/20/99	DR
B	ECO 1221	04/21/99	DR
C	PR 3677	10/08/99	[illegible]







CONTRACT NO.	
APPROVALS	DATE
DRAWN BY SEIFERT	4/97
CHECKED BY	
APPROVED BY DJL	4/97
NEXT ASSY	

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ASSY PCI (GPS)

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		560-5901	C

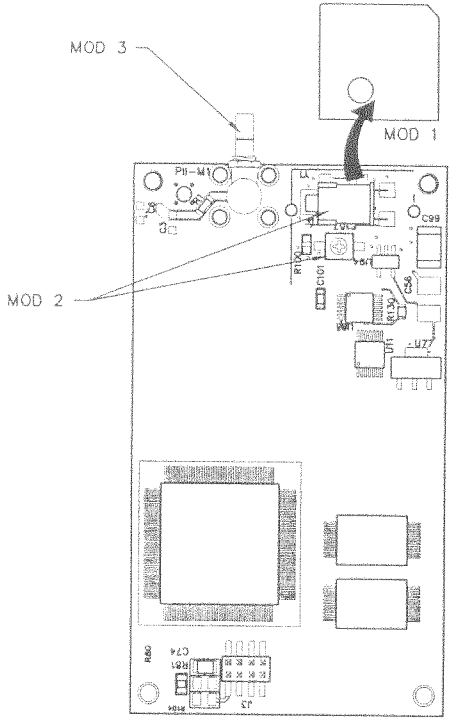
SCALE NONE | SHEET 1 OF 1

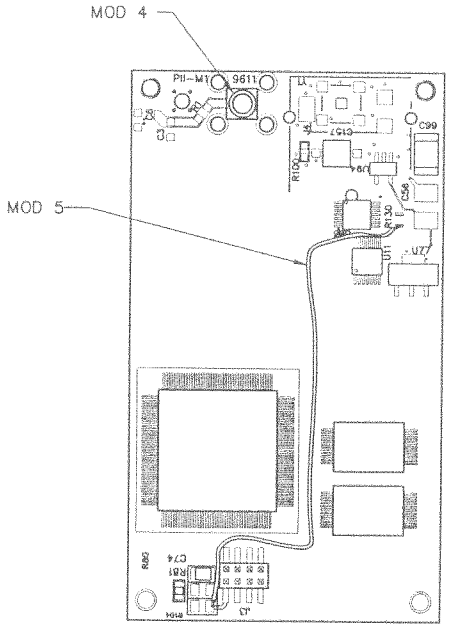
FILENAME: \560\5901
DATE: 10-08-99

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

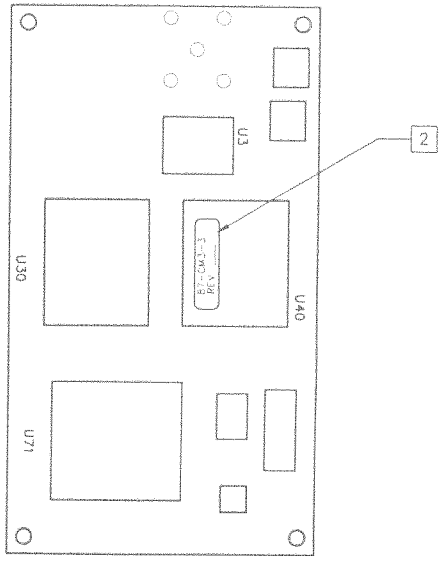
PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5901	ASSY PCI GPS					EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		MSM 10/07/99
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV C (10-07-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		560-5901 REV C
0001-PRINT	REFERENCE PRINT		000000		1.0000	EA		SEE 560-5900
240-002-002	SCREW PHMS 2-56 X 1/4 SS		000000		3.0000	EA		03
252-002	NUT HEX SS 2-56	2-56 HEX	000000		3.0000	EA		04
254-002	WSHR SPLIT #2	#2 LOCKWASHER	000000		3.0000	EA		05
255-002-002	SPCR HEX AL M-F 2-56X1/4	RAF 4501-256-A	000000		3.0000	EA		06
274-008	PLUG HOLE NY .437 DIA.	TROMPETER HP-437	000000		0	EA		REMOVE
375-024	CONN BNC RT ANG JK PC MT	AMP 413631-1	000000		1.0000	EA		J3
381-014	CONN MCX PLUG VERT PC MT	M/A-COM 5863-0000-10	000000		1.0000	EA		J4
400-078	LABEL,FCC (PCI-SG)	MADE FROM 400-082	000000		0	EA		REMOVE/REPLACE W/400-079
400-079	LABEL,FCC (GPS-PCI)	MADE FROM 400-082	000000		1.0000	EA		SEE DWG FOR LOCATION
403-000LP	JUMPER FEMALE LOW PROFILE	SAMTEC SNT-100-BK-T	000000		1.0000	EA		JP3 PIN 2-3
560-5900	ASSY PCB PCI (BASIC)	MADE FROM 560-2900	000000		1.0000	EA		01
87-CM3-3	CORE MODULE MOD		000000		1.0000	EA		02
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		
	INSTALL/MARK LABEL FOR THE PHASE DELAY AT THE 560-5900 FINAL TEST LEVEL (AT TRUETIME).							
NOTE 2			000000		1.0000	EA		
	THE CE IS INSTALLED AT THE 560-5900 LEVEL.							

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	BYPASSED U94	03/05/98	
B	CAR 971	06/24/98	MK





TOP VIEW



BOTTOM VIEW

[2] APPLY P/N REV LABEL WHERE SHOWN.

1. MODIFY 345-CM3 AS FOLLOWS:

MOD 1. REMOVE OSCILLATOR SHIELD.

MOD 2. REMOVE XTAL Y1, TRIMMER CAP C157, AND R130.

MOD 3. REMOVE SMB J1.

MOD 4. INSTALL MCX 381-015 IN J1 ON SIDE SHOWN.

MOD 5. ADD 30 AWG PRELEG WIRE (OR EQUIVALENT) FROM R104 PAD (CLOSEST TO J3) TO R130 PAD.

NOTES: UNLESS OTHERWISE SPECIFIED

CONTRACT NO,	
APPROVALS	DATE
DRAWN BY SEIFERT	4/97
CHECKED BY	
APPROVED BY MK	9/98
NEXT ASSY	

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CORE MODULE MODIFIED

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		87-CM3-3	B

SCALE NONE SHEET 1 OF 1

FILENAME: \87\CM3-3
DATE: 09-17-98

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

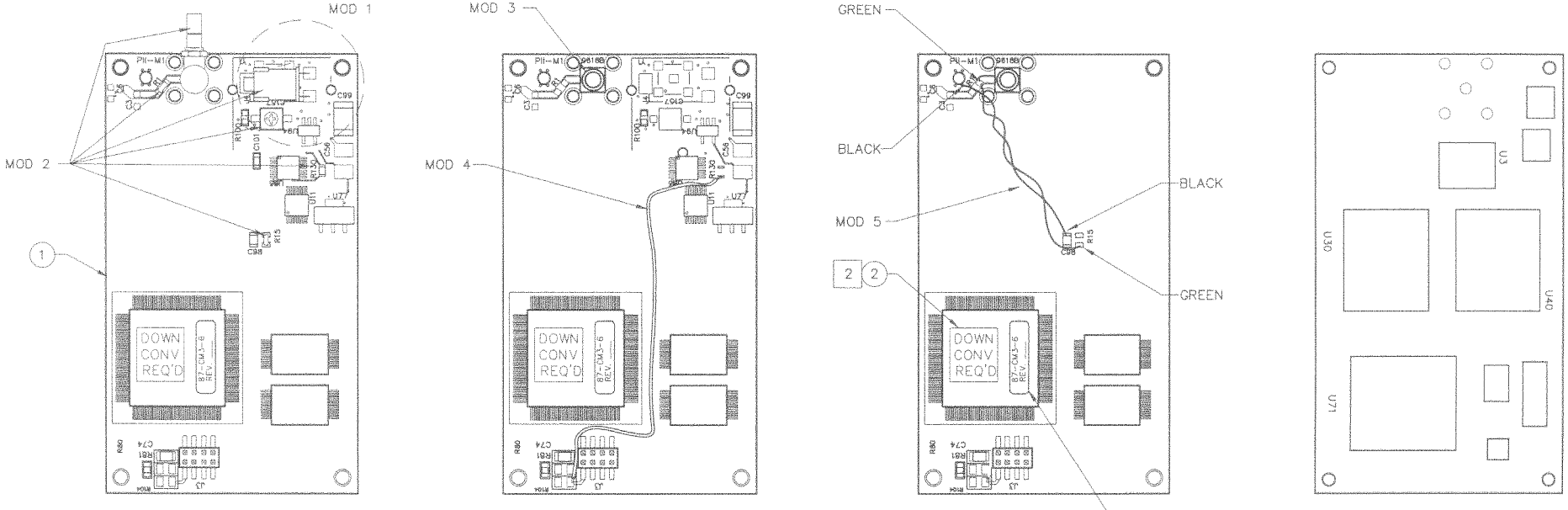
PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
87-CM3-3	CORE MODULE MOD	PCI GPS				EA		
0000-APPROVAL	PARTS LIST APPROVAL		0000		1.0000	EA		JCM 7-16-98
0000-PL	PARTS LIST REV LEVEL		0000		1.0000	EA		REV B (07-15-98)
0000-PRINT	REFERENCE PRINT		0000		1.0000	EA		87-CM3-3 REV B
345-CM3	CORE MODULE 3 (SVEESIX)	TRIMBLE 34055-61	0000		1.0000	EA		
381-015	CONN MCX JACK VERT PC MT	M/A-COM OSX 5862-5002-10	0000		1.0000	EA		J1 (SEE NOTE ON DWG)
400-020	LABEL, EPROM 1/4 X 5/8 IN	BRADY, ECL-107-619	0000		0.0010	BX		
	MARK LABEL WITH 87-CM3-3 AND REVISION AND ADHERE TO CORE MODULE (SEE BOTTOM VIEW ON DWG).							
LA	LABOR ASSEMBLY COST HRS		0000		0	EA		
LT	LABOR TEST COST HOURS		0000		0	EA		

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
560-5901-1	ASSY PCI (GPS)/DN CONV					EA		
								SR 4/99
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV B (04-21-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		SEE 560-5901
0001-PRINT	REFERENCE PRINT		000000		1.0000	EA		SEE 560-5900
008S-331	RES 330 OHM 1/8W 0805	NIC NRC12R331TR	000000		1.0000	EA		R80
036S-NP0220	CAP 22PF NPO 100V 0805 5%	NIC NMC0805NP0220J100TR	000000		0	EA		C52 REMOVE
036S-X7R104-50	CAP .1UF X7R 50V 0805 10%	NIC NMC0805X7R104K50TR	000000		1.0000	EA		C51
240-002-002	SCREW PHMS 2-56 X 1/4 SS		000000		3.0000	EA		03
252-002	NUT HEX SS 2-56	2-56 HEX	000000		3.0000	EA		04
254-002	WSHR SPLIT #2	#2 LOCKWASHER	000000		3.0000	EA		05
255-002-002	SPCR HEX AL M-F 2-56X1/4	RAF 4501-256-A	000000		3.0000	EA		Q6
274-008	PLUG HOLE NY .437 DIA.	TROMPETER HP-437	000000		0	EA		REMOVE
375-024	CONN BNC RT ANG JK PC MT	AMP 413631-1	000000		1.0000	EA		J3
381-014	CONN MCX PLUG VERT PC MT	M/A-COM 5863-0000-10	000000		1.0000	EA		J4
403-000LP	JUMPER FEMALE LOW PROFILE	SAMTEC SNT-100-BK-T	000000		1.0000	EA		JP3 PIN 3-4
560-5900	ASSY PCB PCI (BASIC)	MADE FROM 560-2900	000000		1.0000	EA		01
87-CM3-4	CORE MODULE MOD	PCI GPS/DN CONV	000000		1.0000	EA		02
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		

CE, FCC AND PHASE DELAY LABELS ARE ADDED AT THE 560-5900 LEVEL.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CAR 971	06/25/98	DAA
B	PR 4022	02-25-00	DGK



TOP VIEW

BOTTOM VIEW

3 APPLY P/N REV LABEL WHERE SHOWN.

2 APPLY DOWN CONV LABEL WHERE SHOWN.

1. MODIFY 345-CM3 AS FOLLOWS:

MOD 1 REMOVE OSCILLATOR SHIELD.

MOD 2 REMOVE XTAL Y1, TRIMMER CAP C157, R1, R15, R130 AND J1.

MOD 3 INSTALL MCX 381-015 IN J1 ON SIDE SHOWN.

MOD 4 ADD 30 AWG PRELEG WIRE FROM R130 PAD TO R104 PAD (CLOSEST TO J3-1).

MOD 5 SOLDER TWISTED PAIR (30 AWG BLACK & GREEN) AS FOLLOWS:
a) GREEN FROM R15 TO R1 (CENTER CONDUCTOR OF J1)
b) BLACK FROM J2 (GROUND) TO C98 AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

FILENAME: \87\CM3-4
DATE: 02-25-00

CONTRACT NO,	
APPROVALS	DATE
DRAWN BY RKLEIN	4/98
CHECKED BY	
APPROVED BY DAA	4/98
NEXT ASSY	

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CORE MODULE MODIFIED

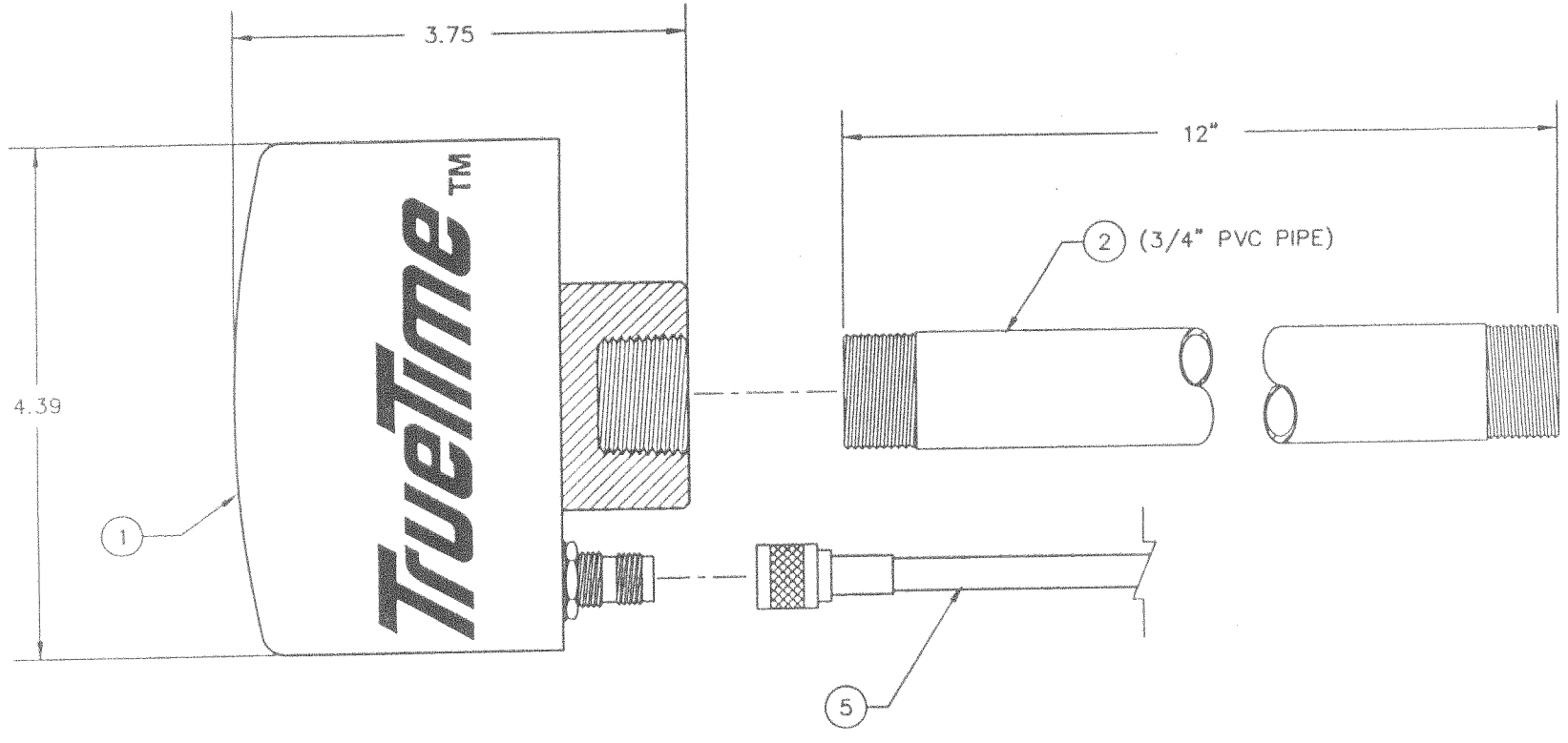
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		87-CM3-4	B

SCALE NONE SHEET 1 OF 1

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
87-CM3-4	CORE MODULE MOD	PCI GPS/DN CONV				EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		DGK 3-1-00
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV B (03-01-00)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		87-CM3-4 REV B
345-CM3XT	CORE MODULE 3 EXT TEMP	TRIMBLE 34057-61	000000		1.0000	EA		01
381-015	CONN MCX JACK VERT PC MT	M/A-COM 5862-5002-10	000000		1.0000	EA		J1 (SEE NOTE ON DWG)
400-019	LABEL, DOWN CONVERTER		000000		1.0000	EA		02
400-020	LABEL, EPROM 1/4 X 5/8 IN	BRADY, ECL-107-619	000000		0.0010	BX		
	MARK LABEL WITH 87-CM3-4 AND REVISION AND ADHERE TO CORE MODULE (SEE TOP VIEWS ON DWG).							
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.	
APPROVALS	DATE
DRAWN BY RNR	11/98
CHECKED BY	
APPROVED BY	1/99
NEXT ASSY	

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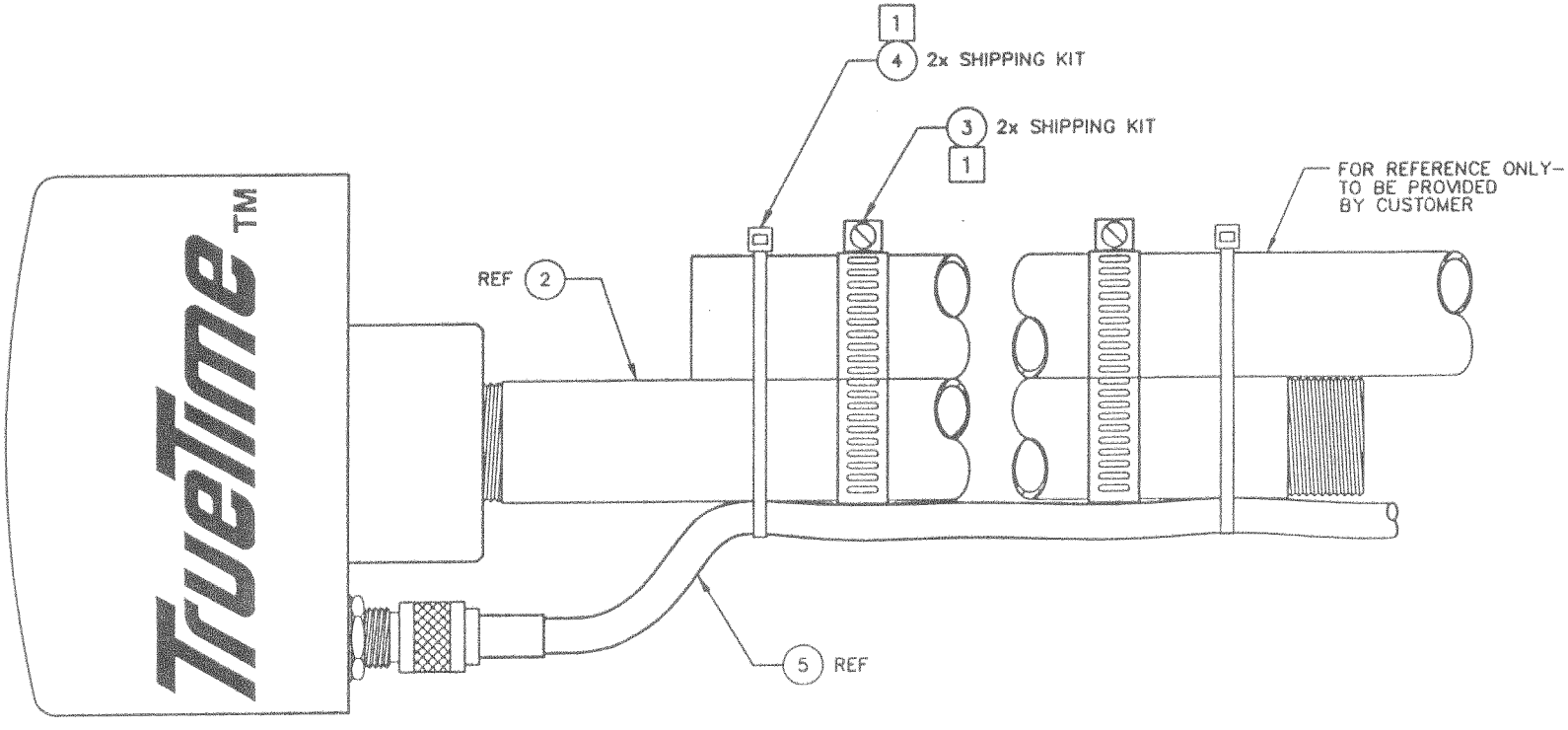
ASSY, ANTENNA DOWN CONVERTER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		142-603	N/C

SCALE NONE SHEET 1 OF 2

FILENAME: \100\42-603A
DATE: 01-12-99



[1] ATTACH ANTENNA SHAFT (ITEM 2) TO CUSTOMER PROVIDED MAST USING CLAMPS (ITEM 3) BEFORE ATTACHING ANTENNA CABLE (ITEM 5) USING TIE WRAPS (ITEM 4).

NOTES: UNLESS OTHERWISE SPECIFIED

FILENAME: \100\42-6038
DATE: 01-12-99

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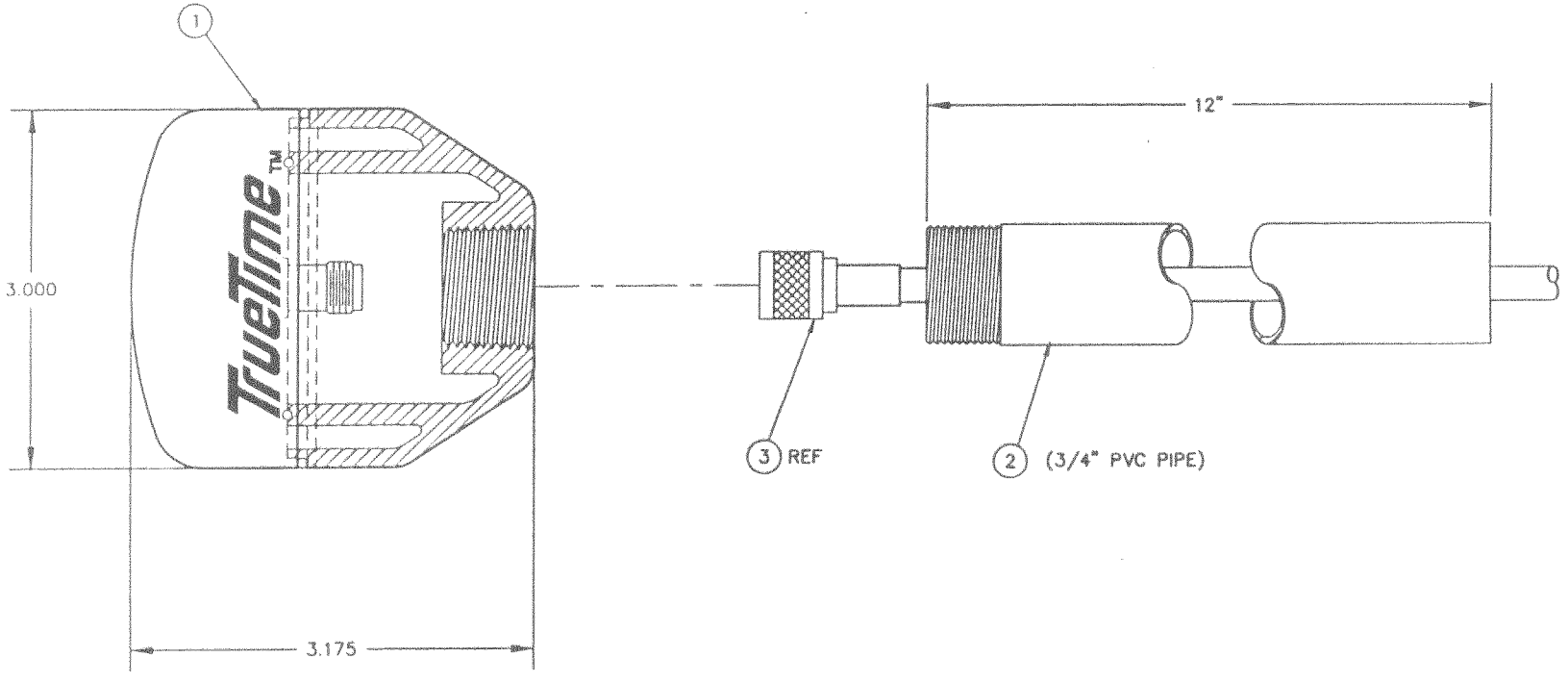
SIZE	CODE IDENT NO	DRAWING NO.	REV
B		142-603	N/C
SCALE NONE			SHEET 2 OF 2

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
142-603	ASSY ANTENNA DN CONVERTER					EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		MDK | ddg 2-8-99
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV N/C (02-08-99)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		142-603 REV N/C
140-016	SHAFT,12 IN. X 3/4 IN.PVC	DARK GREY, THREADED	000000		1.0000	EA		02
140-610	INTEGRATED GPS DN CONVTR	STARLINK IGD ANTENNA	000000		1.0000	EA		01
230-001	CLAMP ANTENNA	IDEAL (SIZE 64)	000000		2.0000	EA		03 SHIPPING KIT
232-001	TIE WIRE 2IN DIA 8IN LONG	PANDUIT PLT2M-M	000000		2.0000	EA		04 SHIPPING KIT
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		

ITEM 05 CABLE SPECIFIED ON SALES ORDER

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



1. TO CONNECT CABLE DISASSEMBLE ANTENNA HOUSING BY REMOVING THE 4 SCREWS TO ACCESS THE TNC CONNECTOR.

NOTES: UNLESS OTHERWISE SPECIFIED

CONTRACT NO,		
APPROVALS		DATE
DRAWN BY	RNR	11/98
CHECKED BY		
APPROVED BY	MJK	11/98
NEXT ASSY		

FILENAME: \100\42-612A
DATE: 11-23-98

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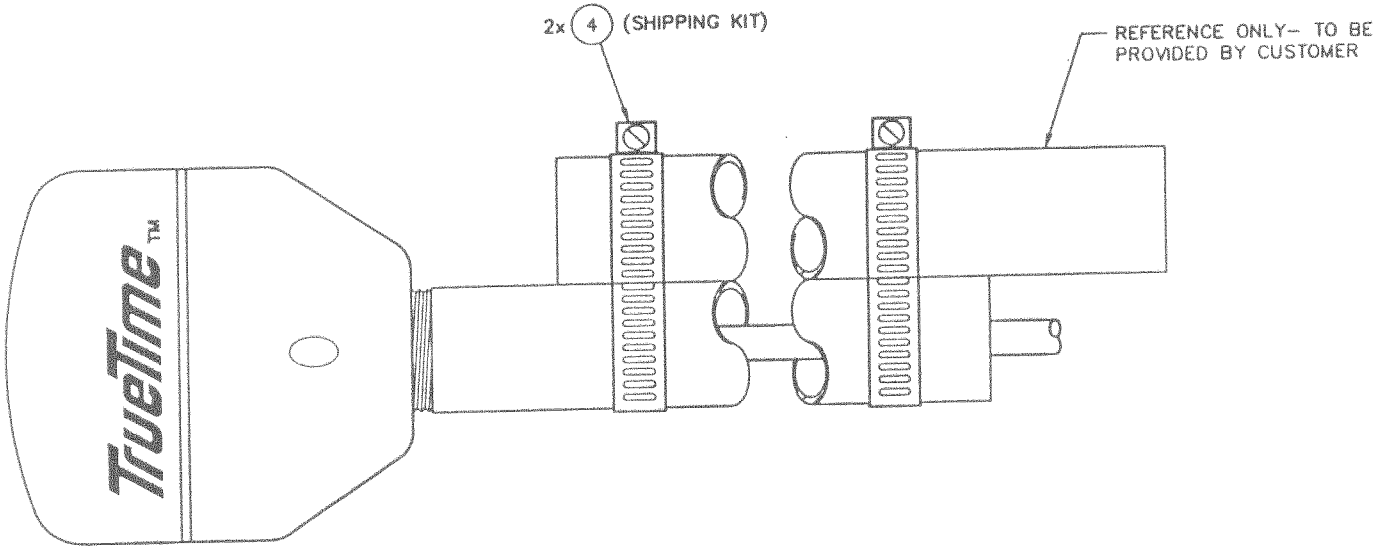
FINAL ASSEMBLY PATCH ANTENNA

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		142-612	N/C

SCALE NONE SHEET 1 OF 2



FILENAME: \100\42-6128
DATE: 11-19-98

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SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		142-612	N/C
SCALE NONE			SHEET 2 OF 2

MAX * BILL OF MATERIALS * SINGLE-LEVEL EXPLOSION BY PART IDENTIFIER W/REFERENCE

PART IDENTIFIER	DESCRIPTION 1	DESCRIPTION 2	EFF DATE	ECN #	QTY/ASSY	UOM	REV LVL	REFERENCE DESCRIPTION
142-612	ASSY ANTENNA PATCH +5V					EA		
0000-APPROVAL	PARTS LIST APPROVAL		000000		1.0000	EA		mc/de 11/98
0000-PL	PARTS LIST REV LEVEL		000000		1.0000	EA		REV N/C (11-24-98)
0000-PRINT	REFERENCE PRINT		000000		1.0000	EA		142-612 REV N/C
140-016	SHAFT,12 IN. X 3/4 IN.PVC	DARK GREY, THREADED	000000		1.0000	EA		02
140-612	ANTENNA GPS 1575MS +5V	AERO AT575-142TT -BOM NAV	000000		1.0000	EA		01
230-001	CLAMP ANTENNA	IDEAL (SIZE 64)	000000		2.0000	EA		04 SHIPPING KIT
LA	LABOR ASSEMBLY COST HRS		000000		0	EA		
LT	LABOR TEST COST HOURS		000000		0	EA		
NOTE 1			000000		1.0000	EA		

ITEM 3 CABLE SPECIFIED ON SALES ORDER.